Product Specification

400GBASE-LR4 10km QSFP-DD Finisar® Transceiver

FTCD4323E2PCL

PRODUCT FEATURES

- Hot-pluggable QSFP-DD type 2 form factor
- Supports 425Gb/s aggregate bit rate
- Power dissipation < 12W
- RoHS-6 compliant
- Case temperature range of 0°C to +70°C
- Single 3.3V power supply
- Maximum link length of 10km on Single Mode Fiber (SMF)
- Aligned with 100G Lambda MSA Group 400G-LR4-10 technical spec
- 4x100Gb/s PAM4 serial lanes
- 8x50G PAM4 retimed 400GAUI-8 electrical interface
- LC duplex receptacle
- I2C management interface

APPLICATIONS

- 400G-LR4-10 applications with FEC

Finisar® FTCD4323E2PCL LR4 QSFP-DD transceiver modules are designed for use in 400 Gigabit Ethernet links on up to 10km of single mode fiber. They are compliant with the QSFP-DD MSA[1], QSFP28 MSA[2], 400G-LR4-10 Technical Specification Rev1.0 Sept 15, 2020[6] and portions of P802.3bs[7]. Digital diagnostic functions are available via the I2C interface, as specified by the QSFP28 MSA and Finisar Application Note AN-21xx[5]. The transceiver is RoHS-6 compliant per Directive 2011/65/EU[3] and Finisar Application Note AN-2038[4].

PRODUCT SELECTION

FTCD4323E2PCL

E: Ethernet protocol
P: Pull-tab type release
C: Commercial temperature range
L: LC duplex receptacle

I. Pin Descriptions

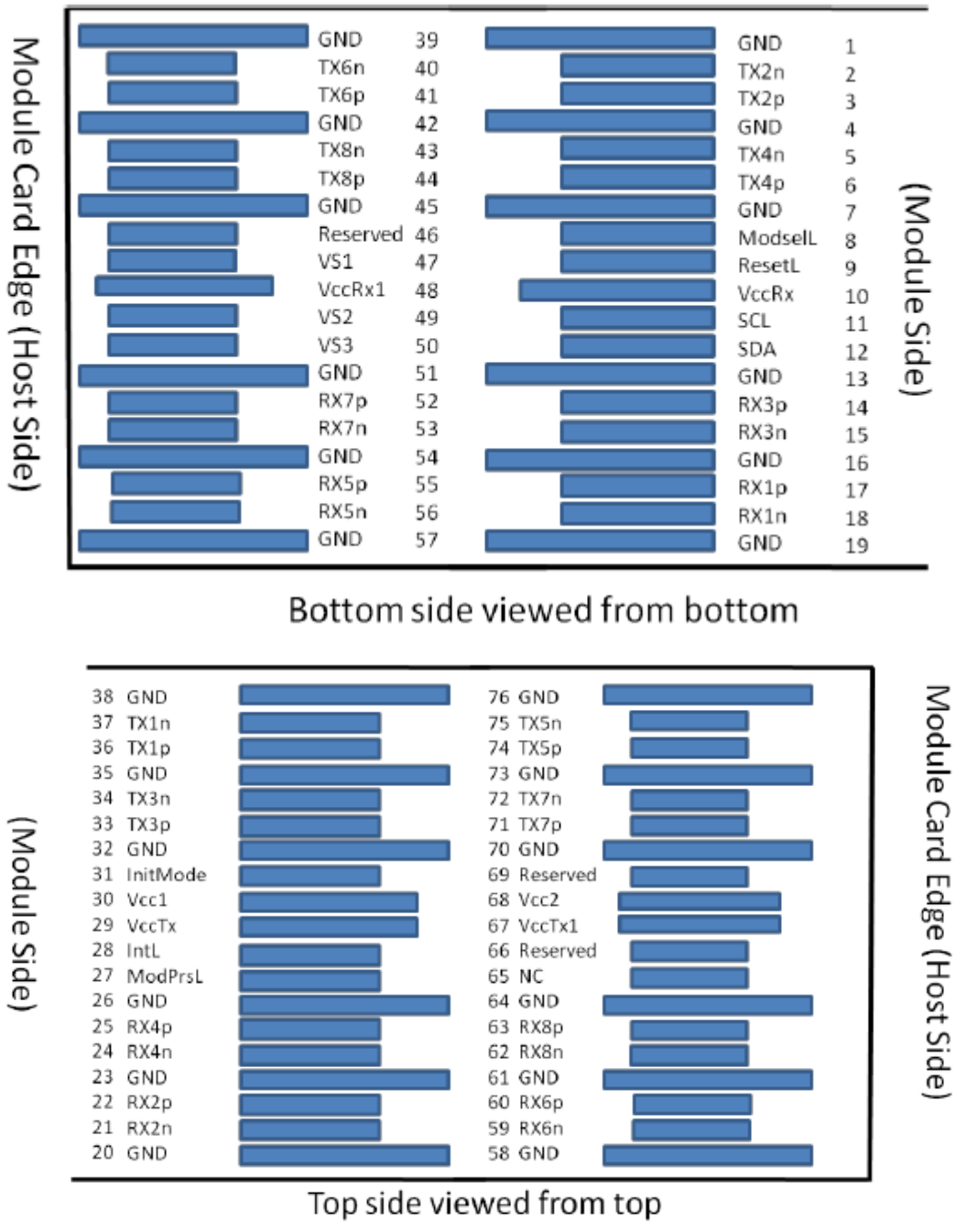

Figure 1 – QSFP-DD -compliant 76-pin connector (per QSFP-DD MSA)

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	

56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

II. Absolute Maximum Ratings

Module performance is not guaranteed beyond the operating range (see Section VI). Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.3		4.0	V	
Storage Temperature	T_S	-40		+85	°C	
Case Operating Temperature	T_{OP}	0		+70	°C	
Relative Humidity	RH	15		85	%	1
Receiver Damage Threshold, per Lane	P_{Rdmg}	5.2			dBm	

Notes:
1. Non-condensing.

III. Electrical Characteristics (EOL, T_{OP} = 0 to +70 °C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			3.83	A	
Module total power	P			12	W	1
Transmitter						
Signaling rate per lane		26.5625± 100 ppm.			Gbd	
Differential data input voltage per lane	Vin,pp,diff	900			mV	2
Differential input return loss		Per equation (83E–5) IEEE802.3bm			dB	
Differential to common mode input return loss		Per equation (83E–6) IEEE802.3bm			dB	
Differential termination mismatch				10	%	
Module stress input test		Per 120E.3.4.1 IEEE802.3bs				3
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode voltage		-350		2850	mV	4
Receiver						
Signaling rate per lane		26.5625± 100 ppm.			Gbd	
AC common-mode output voltage (RMS)				17.5	mV	
Differential output voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Near-end Eye height, differential (min)		70			mV	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Far-end Eye height, differential (min)		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	dB	
Differential output return loss		Per equation 83E-2 IEEE802.3bm				
Common to differential mode conversion return loss		Per equation 83E-3 IEEE802.3bm				
Differential termination mismatch				10	%	
Transition time (min, 20% to 80%)		9.5			ps	
DC common mode voltage (min)		-350		2850	mV	4

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets specified BER
4. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

IV. Optical Characteristics (EOL, TOP = 0 to +70 °C, VCC = 3.135 to 3.465 Volts)

Aligned with 400G-LR4-10 Technical Specification Rev1.0 Sept 15, 2020

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Signaling rate (each lane (range)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelength (range)		1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm	
Side-mode suppression ratio (SMSR)		30			dB	
Total average launch power				11.1	dBm	
Average launch power, each lane				5.1	dBm	
Average launch power, each lane		-2.7			dBm	1
Difference in launch power between any two lanes (OMAouter) max				4	dB	
Outer Optical Modulation Amplitude (OMAouter), each lane max				4.4	dBm	
Outer Optical Modulation Amplitude (OMAouter), each lane min for TDECQ < 1.4 dB for 1.4 dB ≤ TDECQ ≤ 3.9 dB		 0.3 -1.1 + TDECQ			 dBm dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				3.9	dB	
Transmitter eye closure for PAM4 (TECQ), each lane				3.9	dB	
TDECQ – TECQ				2.5	dB	
Average launch power of OFF transmitter, each lane				-16	dBm	
Extinction ratio		3.5			dB	
Transmitter transition time				17	pS	
Transmitter over/under-shoot				25	%	
Transmitter peak-to-peak power				5.2	dBm	
$RIN_{15.6}OMA$				-136	dB/Hz	
Optical return loss tolerance				15.6	dB	
Transmitter reflectance				-26	dB	2

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Receiver						
Signaling rate (each lane (range)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelength (range)		1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm	
Damage threshold, each lane		6.1			dBm	1
Average receive power, each lane				5.1	dBm	
Average receive power, each lane		-9			dBm	2
Receive power (OMAouter), each lane				4.4	dBm	
Difference in receive power between any two lanes (OMAouter)				4.3	dB	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMA_{outer}), each lane (max) for TECQ < 1.4 dB for 1.4 dB ≤ TECQ ≤ 3.9 dB				-6.8 -8.2 + TECQ	dBm dBm	
Stressed receiver sensitivity (OMAouter), each lane				-4.3	dBm	3
Conditions of stressed receiver sensitivity test: [4]						
Stressed eye closure for PAM4 (SECQ), lane under test		3.9			dB	
OMAouter of each aggressor lane		-0.4			dBm	

Notes:
1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
2. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Measured with conformance test signal at TP3 (see 151.8.13) for the BER specified in 151.1.1.
4. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

V. General Product Characteristics

Parameter		Symbol	Min	Typ	Max	Units	Ref.
Bit Rate (all wavelengths combined)		BR			425	Gb/s	
Bit Error Ratio		BER			2.4E-4		1
Maximum Supported Distances							
Fiber Type							
SMF per G.652		Lmax1	0.002		10	km	

Notes:
As defined by IEEE P802.3bs.

VI. Environmental Specifications

Finisar FTCD4323E2PCL LR4 QSFP-DD transceivers have an operating case temperature range of 0°C to +70°C.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	0		+70	°C	
Storage Temperature	T_{sto}	-40		+85	°C	

VII. Regulatory Compliance

Finisar FTCD4323E2PCL LR4 QSFP-DD transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 56
Laser Eye Safety	UL	IEC 60825-1:2014 IEC 60825-2: 2004+A1+A2
Electrical Safety	UL	IEC 62368-1:2018
Electrical Safety	UL/CSA	CLASS 3862.07 CLASS 3862.87

Copies of the referenced certificates are available at Finisar Corporation upon request.

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

VIII. Digital Diagnostics Functions

FTCD4323E2PCL LR4 QSFP-DD transceivers support the I2C-based diagnostics interface specified by the SFF Commitee[1]. See also Finisar Application Note AN-21xx[5] (TBD).

IX. Memory Contents

Per QSFP-DD MSA Specification[1]. See Finisar Application Note AN-21xx[5] (TBD).

X. Mechanical Specifications

Finisar FTCD4323E2PCL LR4-10 QSFP-DD transceivers are compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.

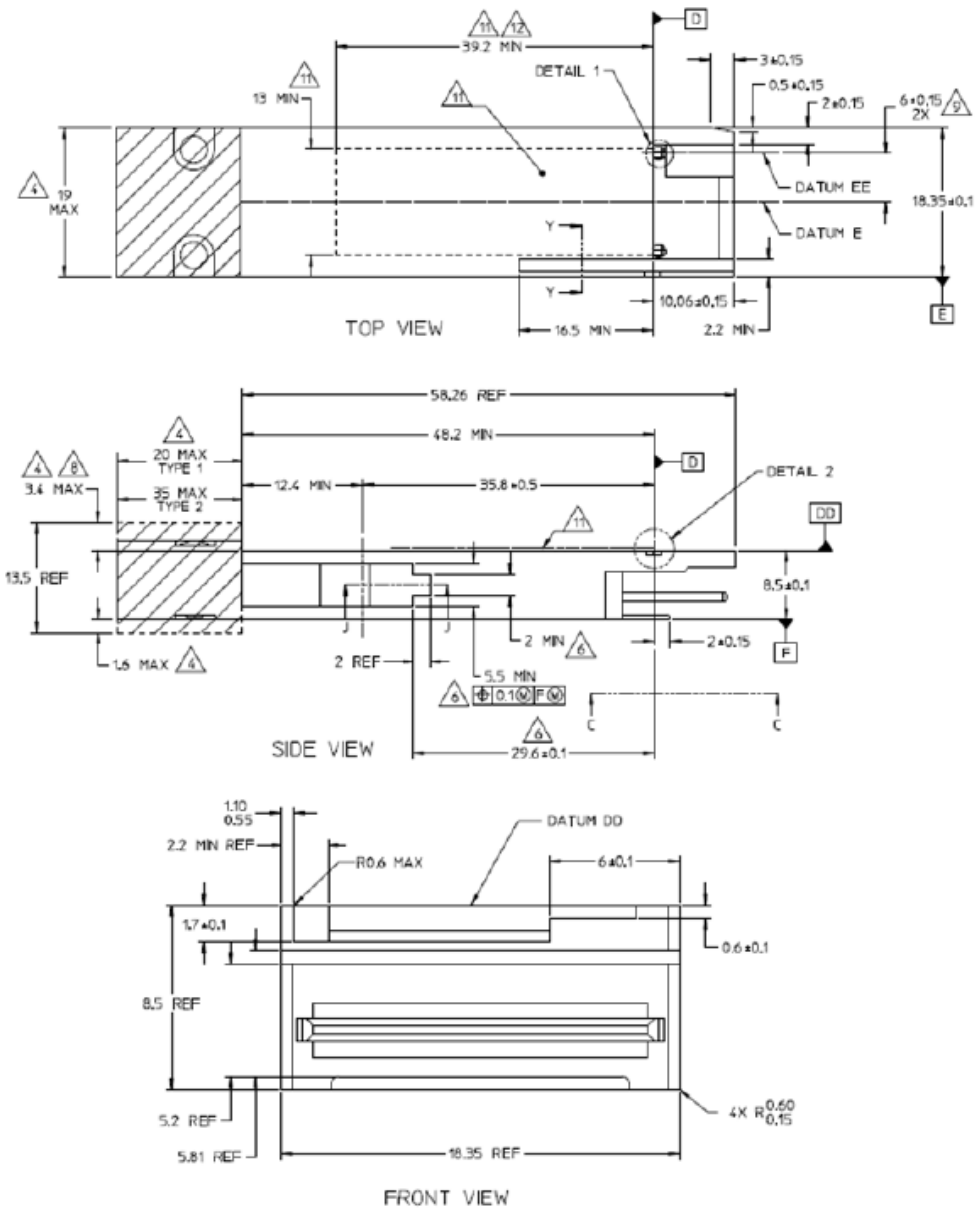

Figure 2 – **FTCD4323E2PCL Mechanical Dimensions.**

Figure 3 – Product Label (Not to Scale)

XI. References

1. QSFP-DD Specification for QSFP Double Density 8X Pluggable Transceiver

2. SFF-8665: "QSFP+ 28Gb/s 4X Pluggable Transceiver Solution (QSFP28)", Rev 1.9, June 29, 2015 and associated SFF documents referenced therein:
    i. SFF-8661
    ii. SFF-8679
    iii. SFF-8636
    iv. SFF-8662
    v. SFF-8663
    vi. SFF-8672
    vii. SFF-8683

3. Directive 2011/65/EU of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment" as well as Commission Delegated Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU. Certain products may use one or more exemptions as allowed by the Directive.

4. Application Note AN-2038: "II-VI Implementation of RoHS Compliant Transceivers".

5. Application Note AN-21xx, Initialization, Finisar Corporation (TBD).

6. 400G-LR4-10 Technical Specification Rev0.3 July 14, 2020

7. IEEE P802.3bs, 400GAUI-8 Interface.

XII. For More Information

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