RCD Snubber

The transfomer's leakage inductance causes MOSFET drain voltage spikes and excessive ringing on the drain voltage waveform, which affects the output voltage sampling after the primary MOSFET turns off.

The RCD snubber circuit limits the drain voltage spike. Figure 14 shows the RCD snubber circuit.

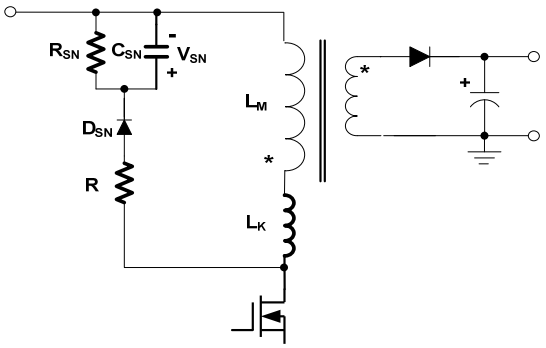


Figure 14: RCD Snubber

Select R_{SN} and C_{SN} to meet the voltage spike requirements and improve system operation.

The power dissipated in the snubber circuit can be approximated with Equation (12):

$$P_{SN} = \frac{1}{2} L_K I_{PK}^2 \frac{V_{SN}}{V_{SN} - N_{PS} V_O} f_S \quad (12)$$

Where L_K is the leakage inductance, V_{SN} is the clamp voltage, and N_{PS} is the turn ratio of the primary-to-secondary side.

Since R_{SN} consumes the majority of the power, calculate R_{SN} with Equation (13):

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}} \quad (13)$$

The maximum ripple of the snubber capacitor voltage is then calculated with Equation (14):

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} R_{SN} f_S} \quad (14)$$

Generally, a 15% ripple is reasonable. The previous equation can also be used to estimate C_{SN}.

Select a time constant ($t = R_{SN} x C_{SN}$) less than 0.1ms for better CV sampling.

The RCD resistor is a trade-off based on the power loss and the acceptable clamp voltage in practical applications.

The damping resistor in series with the RCD has a relatively large value to prevent any excessive voltage ringing that can affect the CV sampling and increase the output ripple. Use a damping resistor value in the range of 100Ω to 500Ω to restrain the drain voltage ringing.

Divided Resistor

For better application performance, select the resistor divider values from 10kΩ to 100kΩ to limit noise from adjacent components on FB. An RC filter can be inserted between the resistor divider and FB to sense purified voltage. The C_{FB} value is recommended to be several pF, and R_{FB} is recommended to be between 1kΩ and 2kΩ. R_{FB} can also limit substrate injection current effects (see Figure 15).

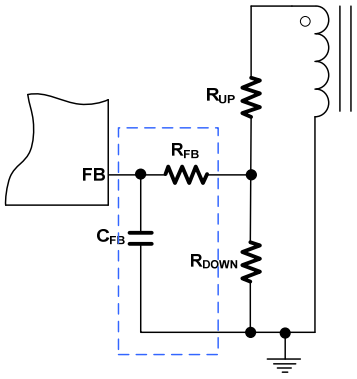


Figure 15: Feedback Resistor Divider Circuit

For accurate CV regulation, the accuracy of these feedback resistors should be at least 1%.

Dummy Load

When the system operates without any load, the output voltage rises above normal operation because of the minimum switching frequency limitation. Use a dummy load for good load regulation. The dummy load is a trade-off between efficiency and load regulation. For example, a large dummy load can deteriorate efficiency and the no-load consumption. For most applications, several mWs for a dummy load is reasonable.

Maximum Switching Frequency

The maximum switching frequency should be limited by the sampling point. Figure 7 and EC table show the relationship of R_{CS} and the sampling point. The secondary on time must be longer than the maximum $T_{FBS-Max}$. Calculate T_{S_ON} with Equation (15):

$$T_{S\_ON} = I_{PK} \frac{N_S \cdot L_M}{N_P \cdot (V_O + V_D)} > t_{FBS\_Max} + t_{FB\_SD} \quad (15)$$

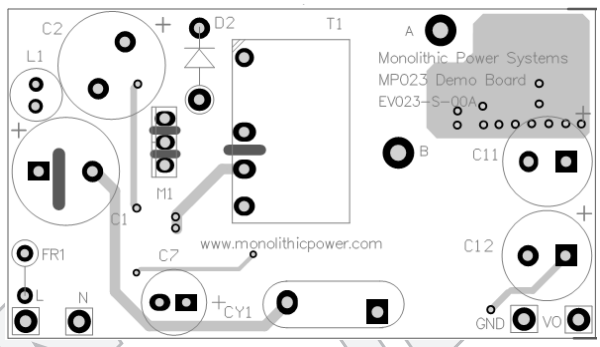
Where $T_{FBS-Max}$ is the FB maximum sampling time, and t_{FB_SD} is the FB sampling duration.

Combine Equation (15) and the relationship of R_{CP} and D_{S-Max} shown in Table 1 to fix the maximum switching frequency.

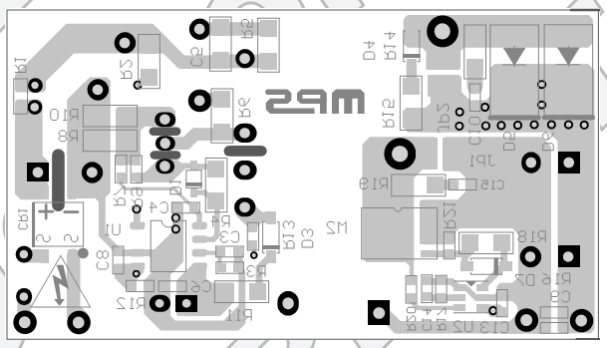
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, good EMI, and good thermal performance. For best results, refer to Figure 16 and follow the guidelines below.

1. Minimize the loop area formed by the input capacitor, the primary transformer winding, the MOSFET drain source, and the sensing resistor to reduce EMI noise.
2. Minimize the voltage jumping area, such as the MOSFET drain, the anode of the secondary diode, etc. for better EMI.
3. Minimize the clamp circuit loop to reduce EMI.
4. Minimize the secondary loop area of the output diode and output filter to reduce EMI noise. Sufficient copper areas should be provided at the cathode terminal of the output diode to act as a heat sink.
5. Place the AC input away from the switching nodes to minimize any noise coupling that may bypass the input filter.
6. Place the bypass capacitor as close to the IC as possible.
7. Place the feedback resistors next to FB and minimize the feedback sampling loop to minimize noise coupling.
8. Use a single-point connection at the negative terminal of the input filter capacitor for the IC GND and bias winding return.



Top Layer



Bottom Layer

Figure 16: Recommended Layout

Design Example

Table 3 is a design example following the application guidelines.

Table 3: Design Example

V_{IN}	85Vac~265Vac 47Hz/63Hz
V_{OUT}	5V
I_{OUT}	2.4A
f_S	70kHz

Figure 17 shows the detailed application schematic. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUIT

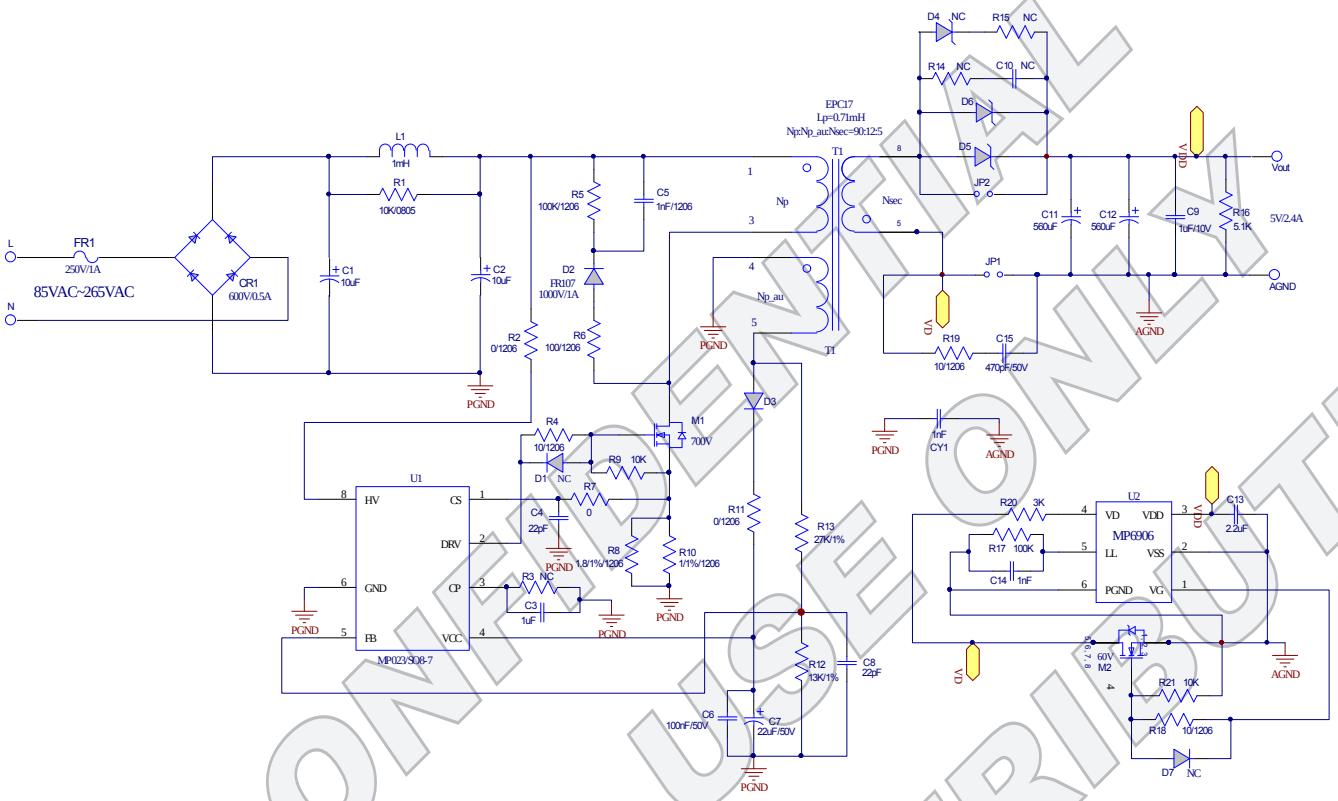
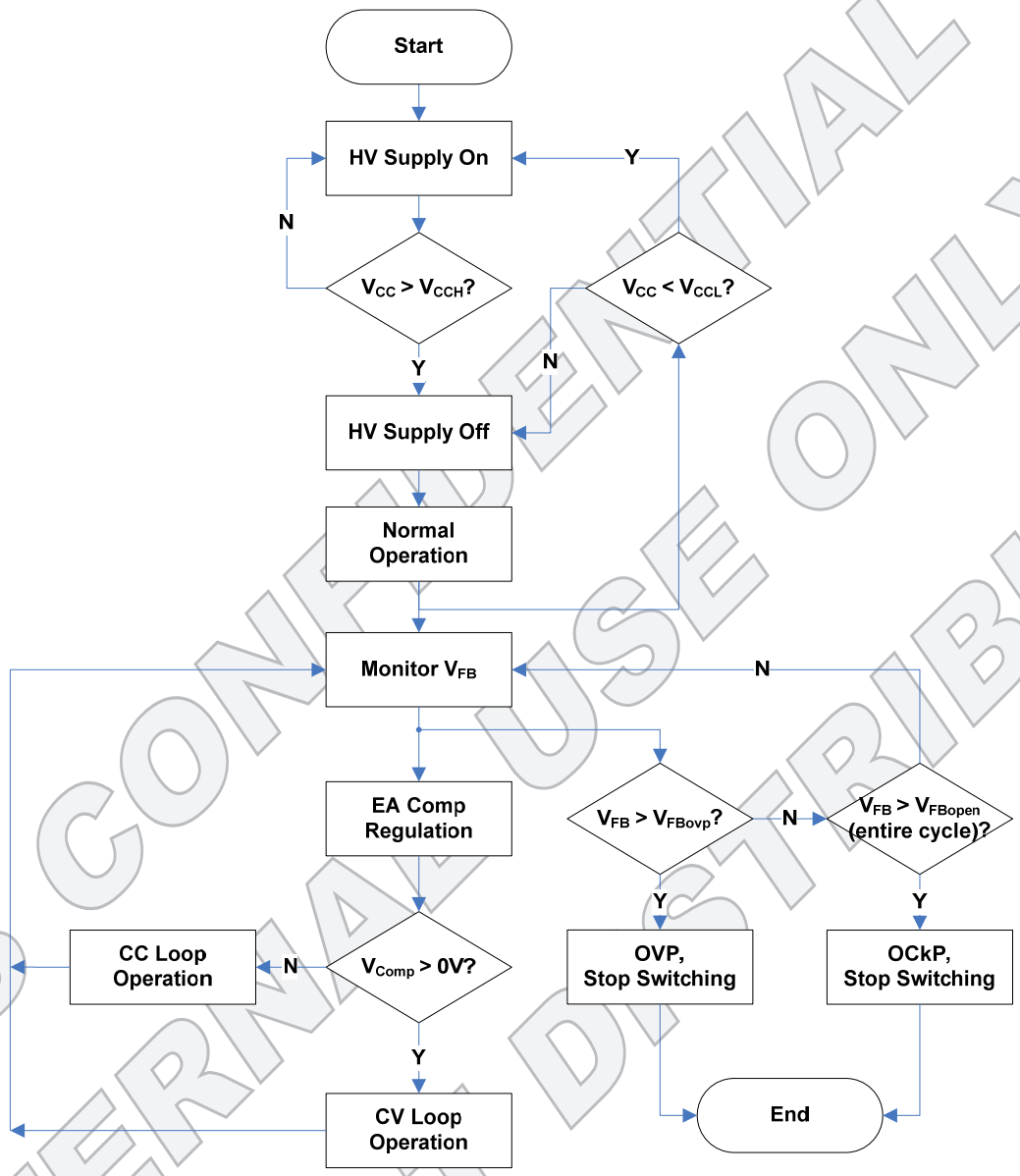
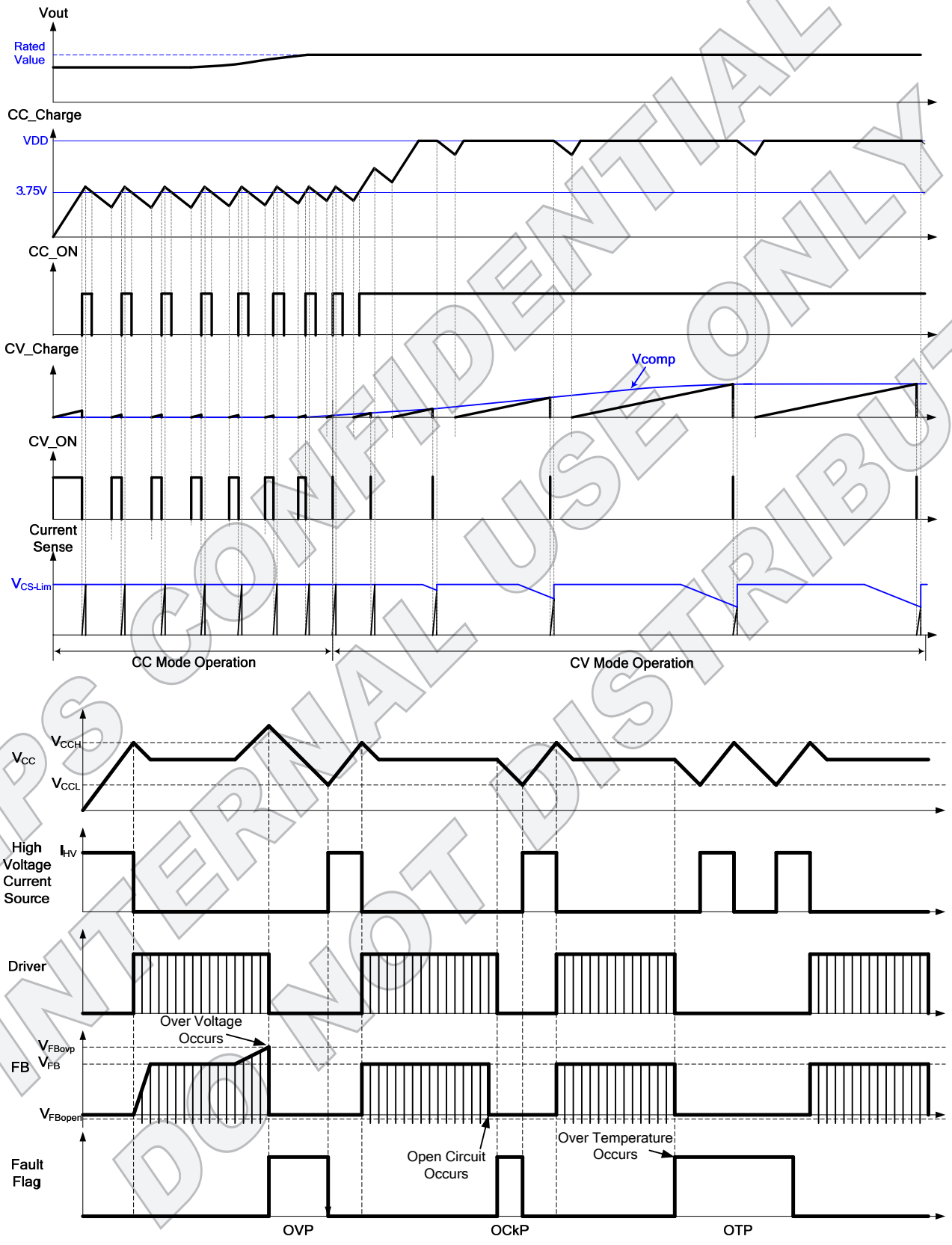


Figure 17: Typical Application—Universal Input, 5V/2.4A Output

FLOW CHART

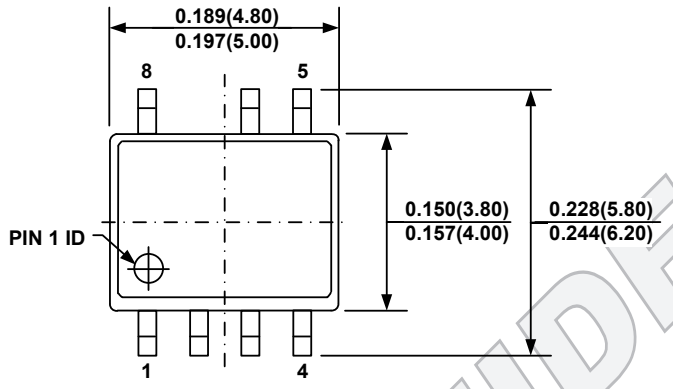


SIGNAL TIMING SEQUENCE WAVEFORMS

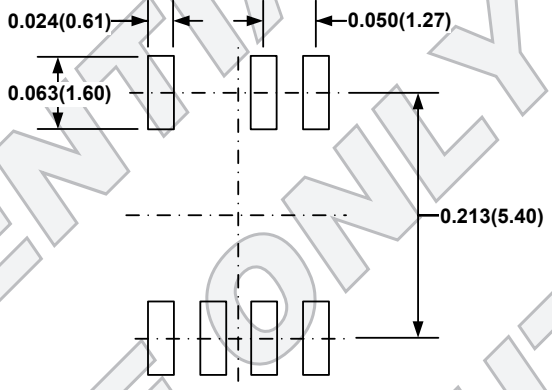


PACKAGE INFORMATION

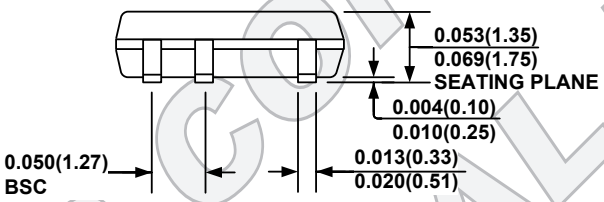
SOIC8-7A



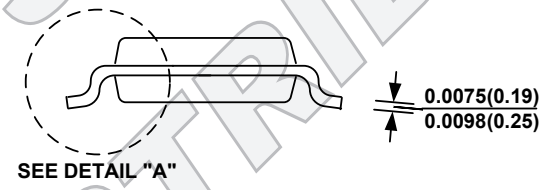
TOP VIEW



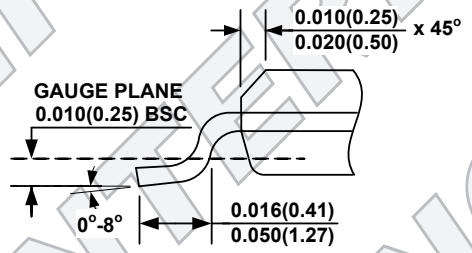
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.