MP2319

3A, 18V, 650kHz, High-Efficiency, Synchronous, Step-Down Converter in 8-Pin TSOT23

The Future of Analog IC Technology

DESCRIPTION

The MP2319 is a fully-integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP2319 offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input range. The MP2319 has synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time control operation provides a very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), over-voltage protection (OVP), and thermal shutdown.

The MP2319 requires a minimal number of readily available, standard, external components and is available in a space-saving, 8-pin, TSOT23 package.

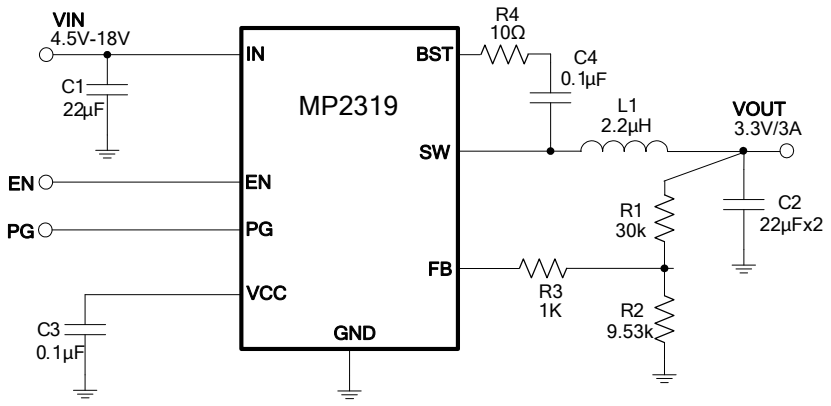
FEATURES

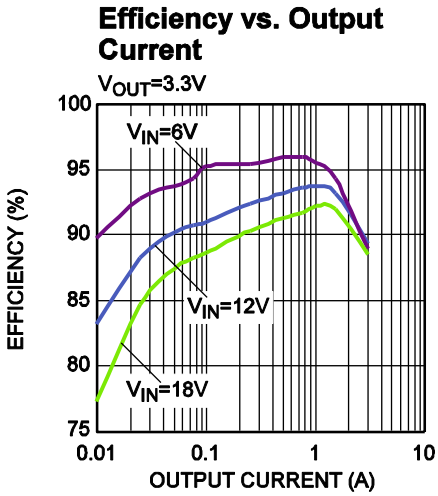
- Wide 4.5V to 18V Operating Input Range
- 3A Output Current
- 105mΩ/57mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Output Adjustable from 0.8V
- EN Shutdown Output Discharge
- Internal Soft Start
- High-Efficiency Synchronous Mode Operation
- Fixed 650kHz Switching Frequency
- EN and Power Good for Power Sequencing
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Auto-Retry Over-Voltage Protection (OVP)
- Available in a TSOT23-8 Package

APPLICATIONS

- Security Cameras
- Portable Devices, xDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purposes

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2319GJ	TSOT23-8	*See Below*

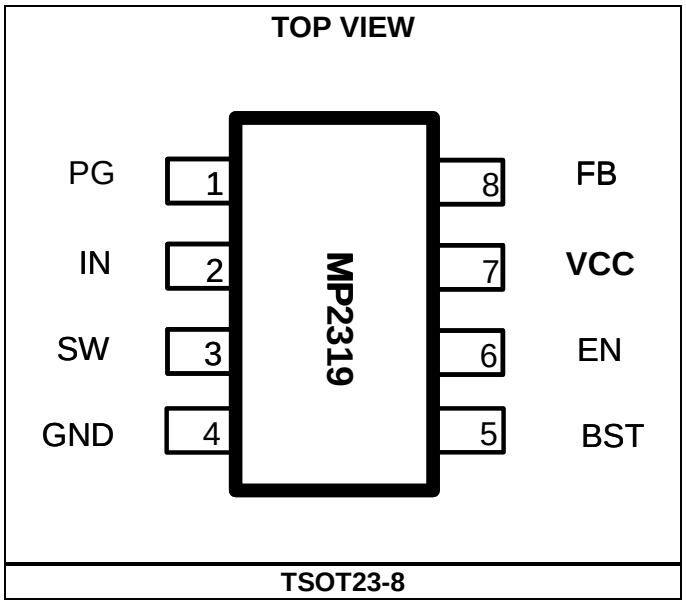
* For Tape & Reel, add suffix –Z (e.g. MP2319GJ–Z)

TOP MARKING

APVY

APV: Product code of MP2319GJ
Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +22V
V_{SW} .... -0.6V (-5V < 10ns) to +22V (23V < 10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{EN} ..... V_{IN}
All other pins ..... -0.3V to +5.5V
Continuous power dissipation (T_A = +25°C) (2)
..... 1.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.5V to 18V
Output voltage (V_{OUT}) ..... 0.8V to 12V
Operating junction temp. ..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-8	100	55	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C[5], unless otherwise noted. Typical value is based on the average value when T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		1.2	5	μA
Supply current (quiescent)	I_q	V_{EN} = 2V, V_{FB} = 0.9V		270	350	μA
MOSFET						
HS switch on resistance	$HS_{RDS(ON)}$	$V_{BST - SW}$ = 5V		105		mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 5V		57		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V/0V			1	μA
Current Limit and ZCD						
Valley current limit	$I_{LIMIT\ VY}$	Duty = 40%	2.8	3.5		A
ZCD	I_{ZCD}			50		mA
Switching Frequency and Minimum On/Off Timer						
Switching frequency	Fs		510	650	790	kHz
Minimum on time[6]	$T_{On\ MIN}$			55		ns
Minimum off time[6]	$T_{Off\ MIN}$			90		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	792	800	808	mV
Feedback voltage	V_{FB}	T_J = -40°C to +125°C	788	800	812	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	50	nA
Soft-start period	t_{SS}	V_{OUT} = 10% to 90%		0.8		ms
Enable (EN) and UVLO						
EN rising threshold	$V_{EN\ RISING}$		1.22	1.285	1.35	V
EN falling hysteresis	$V_{EN\ \_Hys}$			140		mV
EN pull-down resistor	$R_{EN\ PD}$			1.1		MΩ
V_{IN} under-voltage lockout threshold rising	$INUV_{Vth}$		3.4	3.85	4.3	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			670		mV
VCC						
VCC regulator	V_{CC}			5		V
VCC load regulation		I_{CC} = 5mA			3	%
OVP						
OVP rising threshold	$V_{OVP1\ RISE}$		1.18	1.22	1.26	V_{REF}
OVP falling threshold	$V_{OVP\ FALL}$		1.025	1.065	1.105	V_{REF}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C[5], unless otherwise noted. Typical value is based on the average value when T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good UV rising threshold	PG_{vth_Hi}		0.875	0.915	0.955	V_{FB}
Power good UV falling threshold	PG_{vth_Lo}		0.77	0.81	0.85	V_{FB}
Power good OV rising threshold	$PG_{vth\_Hi\_OV}$		1.025	1.065	1.105	V_{FB}
Power good OV falling threshold	$PG_{vth\_Lo\_OV}$		1.18	1.22	1.26	V_{FB}
Power good low to high delay	PG_{Td}			56		µs
Power good high to low delay	PG_{Td}			40		µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V		2.5	10	µA
Thermal Protection						
Thermal shutdown[6]	T_{SD}			150		°C
Thermal hysteresis[6]	$T_{SD\ HYS}$			20		°C

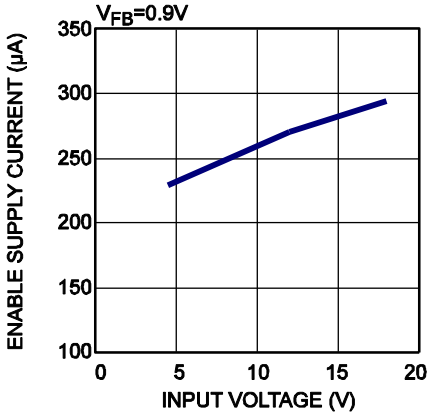
NOTES:

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Guaranteed by design and characterization test.

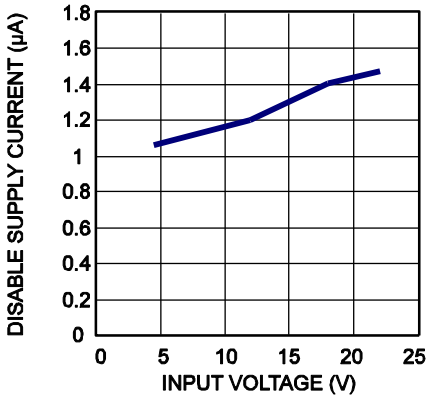
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

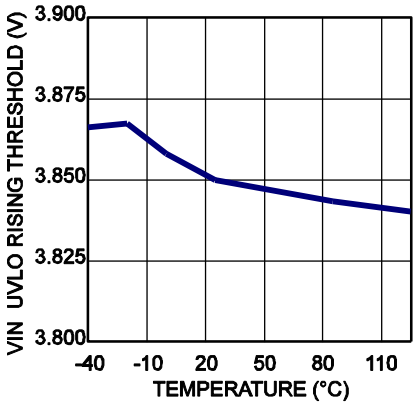
Quiescent Current vs. Input Voltage



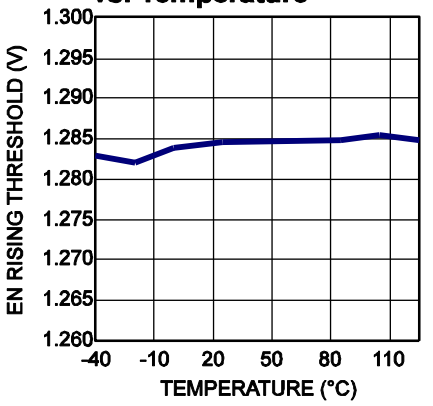
Disabled Supply Current vs. Input Voltage



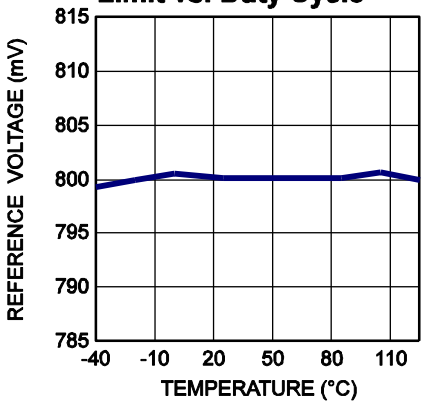
VIN UVLO Rising Threshold vs. Temperature



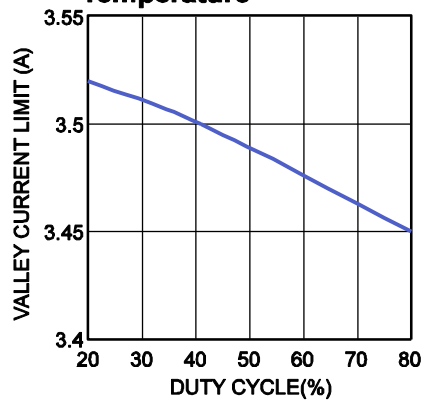
EN Rising Threshold vs. Temperature



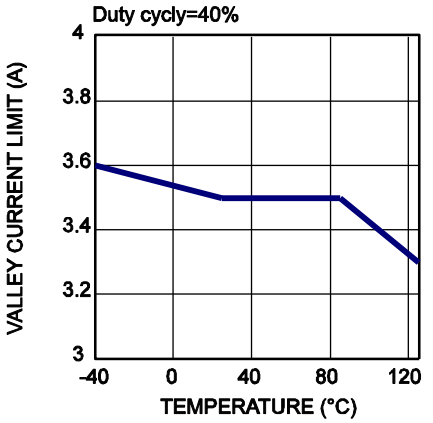
Inductor Valley Current Limit vs. Duty Cycle



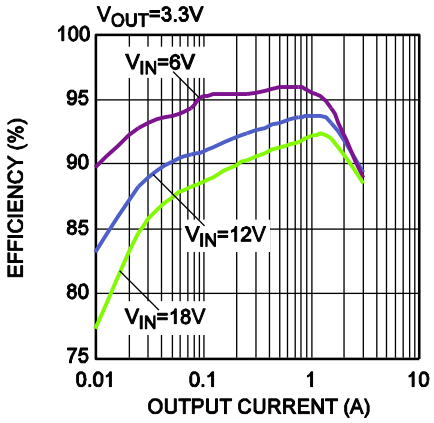
Reference Voltage vs. Temperature



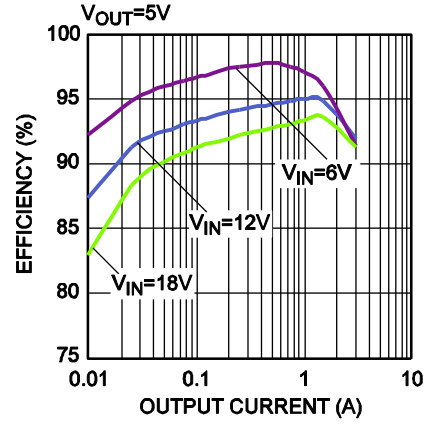
Inductor Valley Current Limit vs. Temperature



Efficiency vs. Output Current



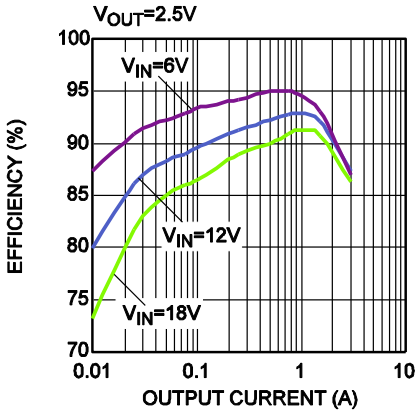
Efficiency vs. Output Current



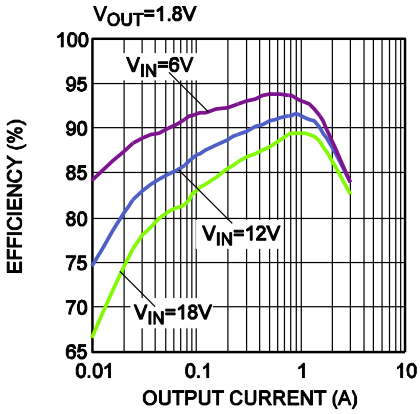
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

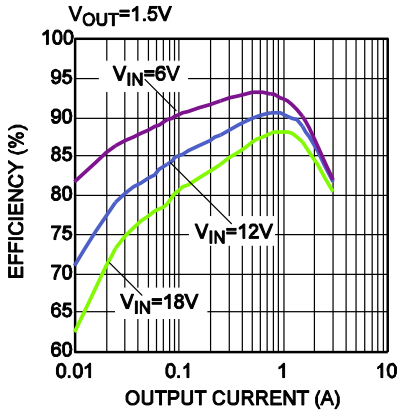
Efficiency vs. Output Current



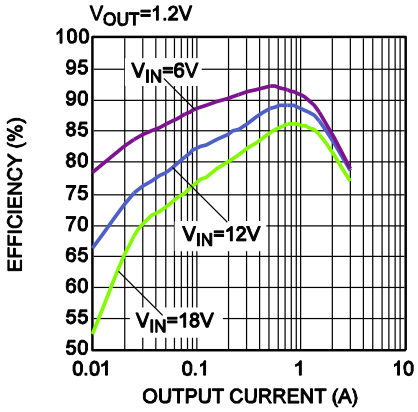
Efficiency vs. Output Current



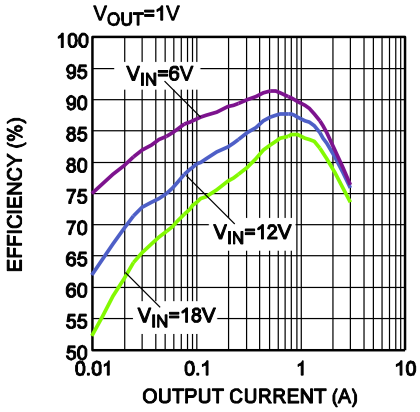
Efficiency vs. Output Current



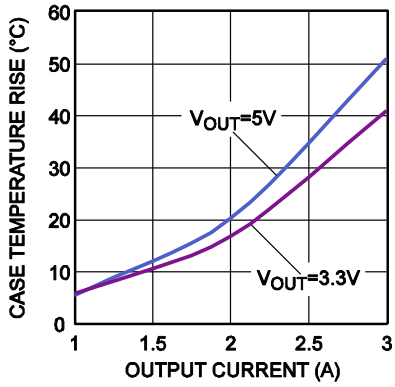
Efficiency vs. Output Current



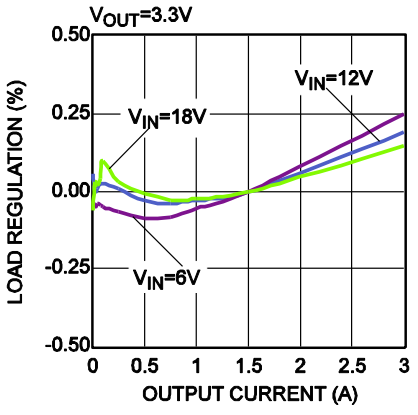
Efficiency vs. Output Current



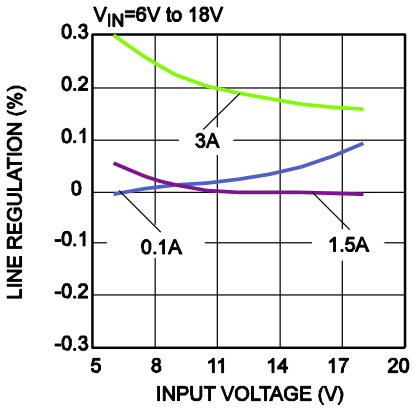
Case Temperature Rise vs. Output Current



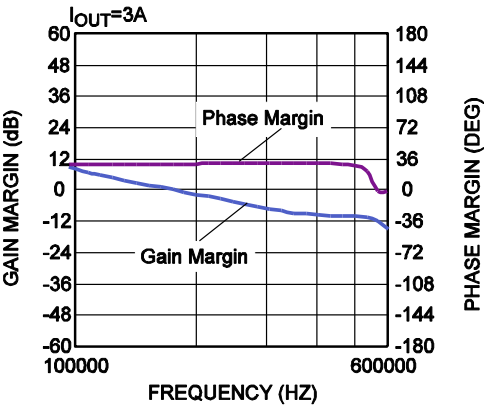
Load Regulation



Line Regulation



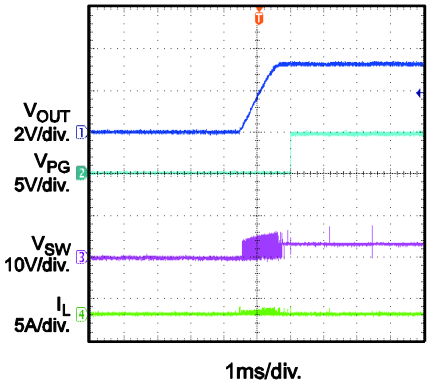
Bode Plot



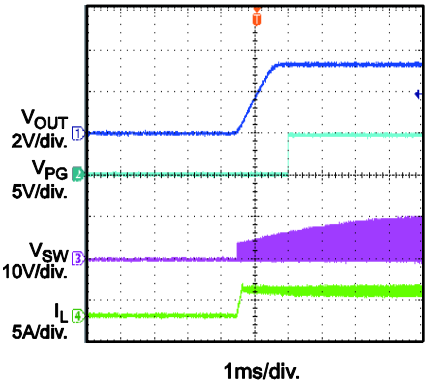
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

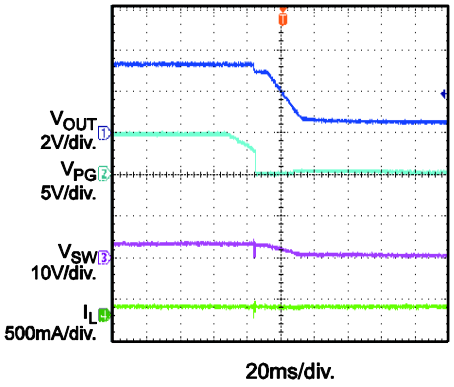
Start-Up through Input Voltage
I_{OUT}=0A



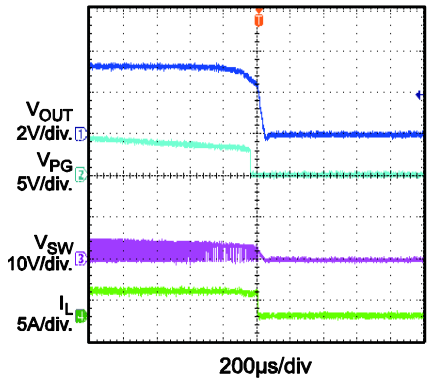
Start-Up through Input Voltage
I_{OUT}=3A



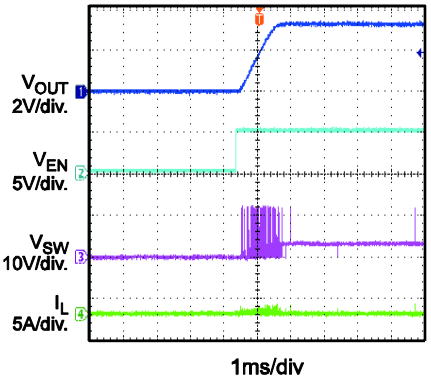
Shutdown through Input Voltage
I_{OUT}=0A



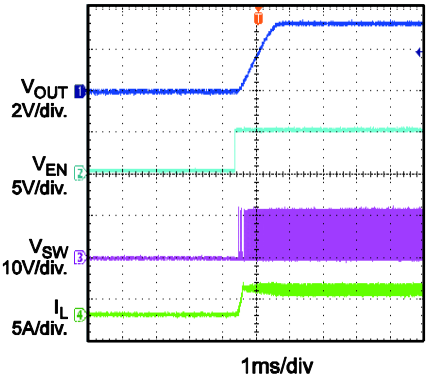
Shutdown through Input Voltage
I_{OUT}=3V



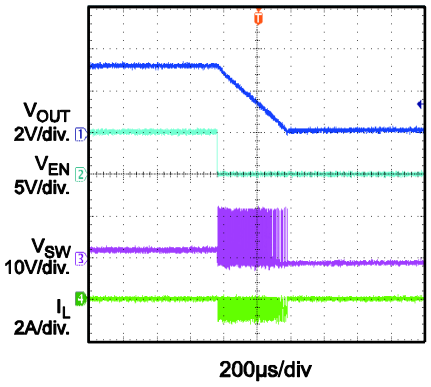
Start-Up through Enable
I_{OUT}=0A



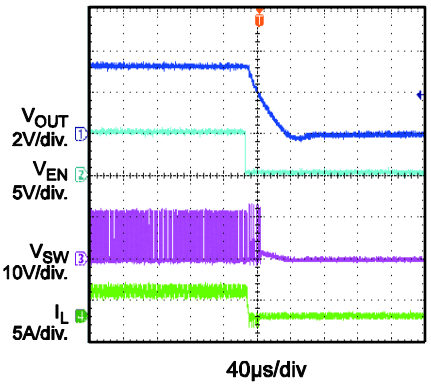
Start-Up through Enable
I_{OUT}=3A



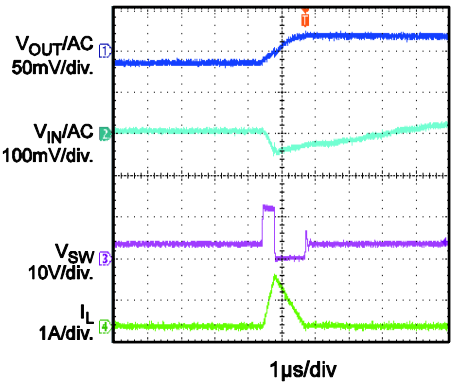
Shutdown through Enable
I_{OUT}=0A



Shutdown through Enable
I_{OUT}=3A



Input/Output Ripple
I_{OUT}=0A

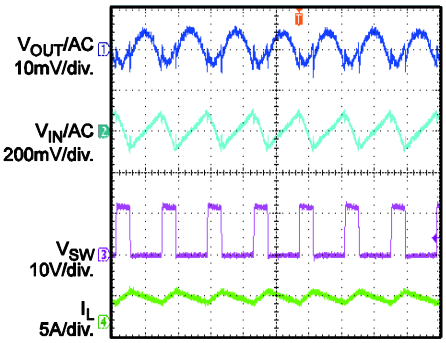


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = 25°C, unless otherwise noted.

Input/Output Ripple

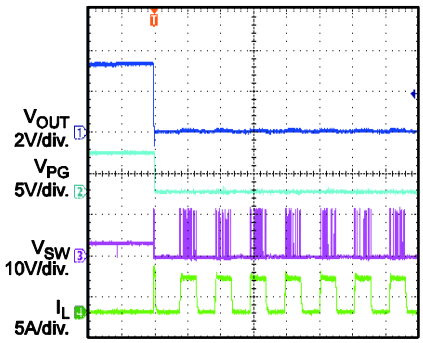
I_{OUT}=3A



1µs/div.

SCP Entry

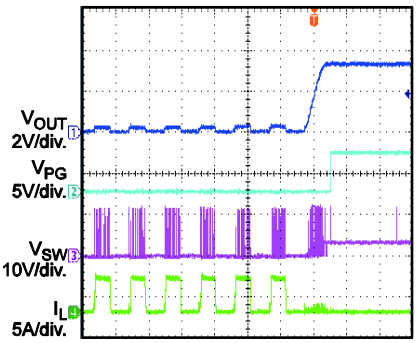
I_{OUT}=0A



2ms/div.

SCP Recovery

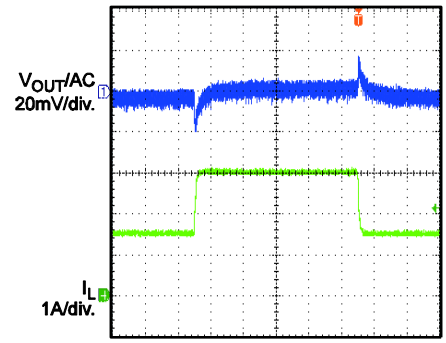
I_{OUT}=0A



2ms/div.

Load Transient Response

I_{OUT}=1.5A to 3A



100µs/div

PIN FUNCTIONS

Package Pin #	Name	Description
1	PG	**Power good output.** The output of PG is an open drain that goes high if the output voltage is within a nominal output window.
2	IN	**Supply voltage.** The MP2319 operates from a 4.5V to 18V input rail. C1 is needed to decouple the input rail. Connect IN using wide PCB traces.
3	SW	**Switch output.** Connect SW using wide PCB traces.
4	GND	**System ground.** GND is the reference ground of the regulated output voltage. GND requires careful consideration during PCB layout. Connect GND with copper traces and vias.
5	BST	**Bootstrap.** Connect a capacitor between SW and BS to form a floating supply across the high-side switch driver. Place a 10Ω resistor between the SW and BST cap to reduce SW voltage spikes.
6	EN	**Enable.** Set EN = 1 to enable the MP2319. When floating, EN is pulled down to GND by an internal 1.1MΩ resistor, and the MP2319 is disabled.
7	VCC	**Internal bias supply.** Decouple VCC with a 0.1µF to 0.22µF capacitor. The capacitor should not exceed 0.22µF. The VCC capacitor should be placed close to VCC and GND.
8	FB	**Feedback.** FB sets the output voltage when connected to the tap of an external resistor divider that is connected between the output and GND.

BLOCK DIAGRAM

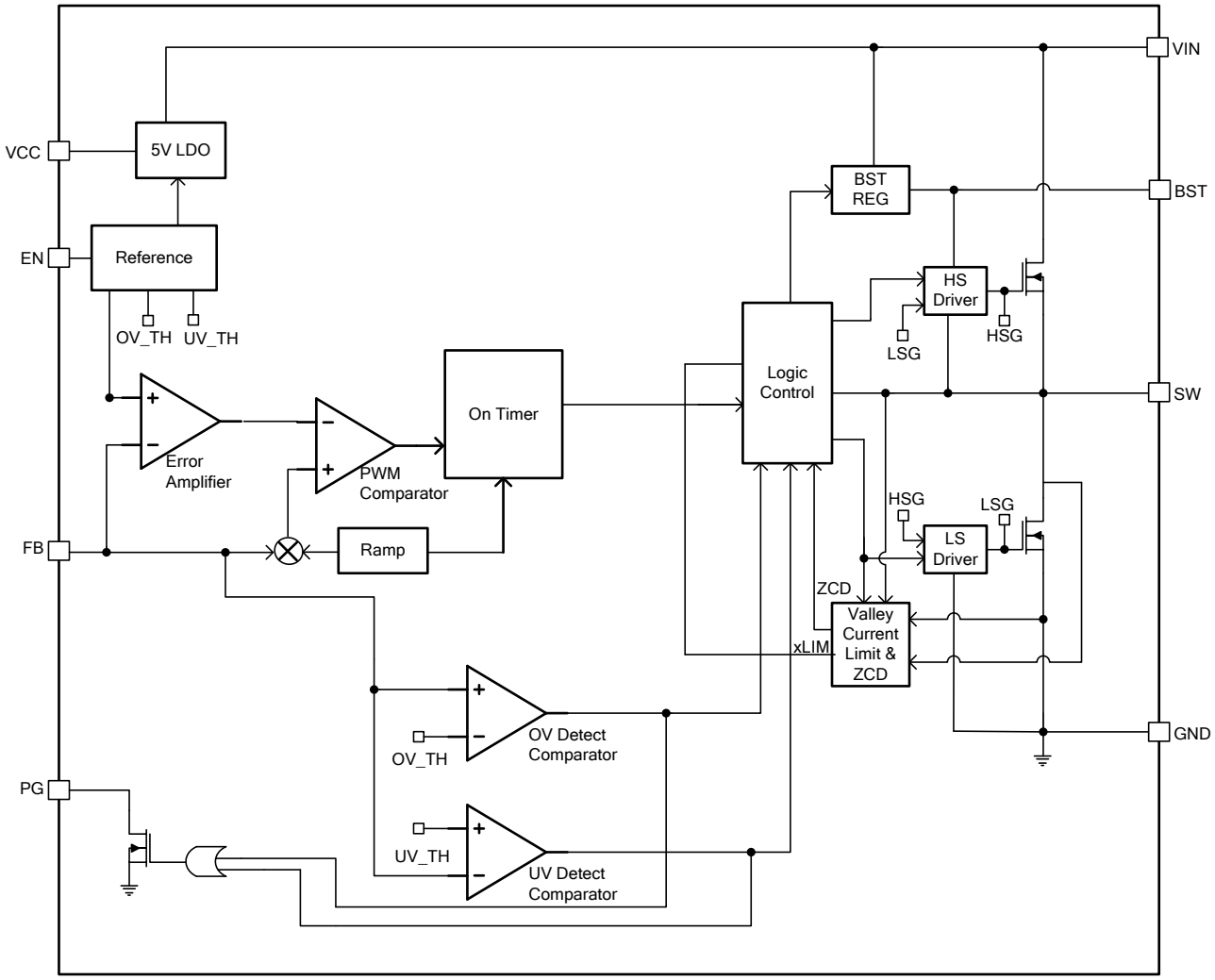


Figure 1: Functional Block Diagram

OPERATION

The MP2319 is fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide a fast transient response and ease loop stabilization. Figure 2 shows the simplified ramp compensation block in the MP2319.

At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off or enters an off state. It is turned on again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called a shoot-through. To prevent a shoot-through, a dead time (DT) is generated internally between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

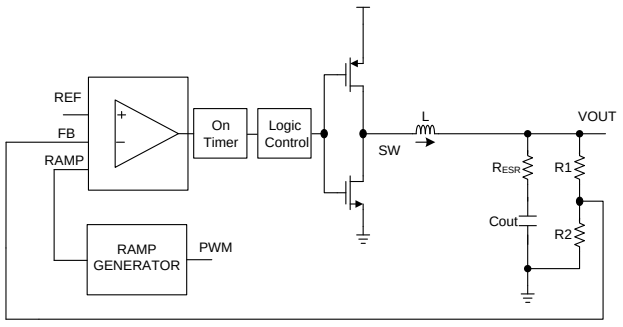


Figure 2: Simplified Ramp Compensation Block

Heavy-Load Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 3). When V_{FB} is below V_{EAO}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period.

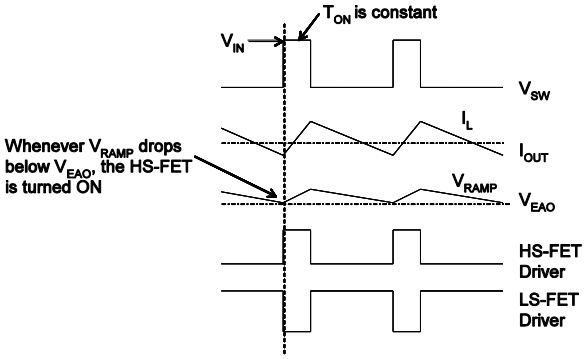


Figure 3: Heavy-Load Operation

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

Light-Load Operation

When the MP2319 works in pulse-frequency modulation (PFM) and light-load operation, the MP2319 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 4). Therefore, the output capacitors discharge slowly to GND through R1 and R2. This operation improves the device efficiency greatly when the output current is low.

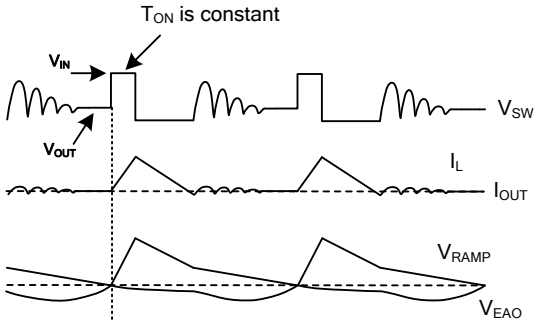


Figure 4: Light-Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does in heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero, and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Enable (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. When floating, EN is pulled down to GND by an internal 1.1MΩ resistor. EN can be connected directly to V_{IN}. EN supports an 18V input range.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2319 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 3.85V, while its falling threshold is 3.18V consistently.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 0.8ms internally.

Power Good (PG) Indicator

The MP2319 uses a power good (PG) output to indicate whether the output voltage of the module is ready or not. PG is an open-drain output. Connect PG to VCC or another voltage source through a pull-up resistor (e.g.: 100kΩ). When input voltage is applied, PG is pulled down to GND before the internal V_{SS} > 1V. After V_{SS} > 1V, when V_{FB} is above 91.5% of V_{REF}, PG is pulled high after a 56µs delay. During normal operation, PG is pulled low when V_{FB} drops below 81% of V_{REF} after a 40µs delay.

When UVLO or OTP occurs, PG is pulled low immediately. When over-current (OC) occurs, PG is pulled low when V_{FB} drops below 81% of V_{REF} after a 40µs delay. PG is pulled low to indicate output over-voltage when V_{FB} rises above 122% of V_{REF} after a 40µs delay. If V_{FB} falls below 105% after over-voltage protection (OVP), PG is pulled high after a 56µs delay.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP2319 has a valley limit control. During the LS-FET on state, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the LS limit comparator (shown in Figure 1) turns over, and the MP2319 enters over-current protection (OCP) mode. The HS-FET waits until the inductor current falls below the valley current limit before turning on again. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold, typically 50% below the reference. Once UV is triggered, the MP2319 enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. The MP2319 disables the output power stage, discharges the soft-start cap, and then tries to soft-start automatically. If the over-current condition still remains after the soft-start ends, the MP2319 repeats this operation cycle until the over-current condition is removed, and then the output rises back to regulation levels. OCP is a non-latch protection.

Over-Voltage Protection (OVP)

The MP2319 monitors the resistor-divided feedback voltage to detect over-voltage (OV). When the feedback voltage rises higher than 122% of the target voltage, the controller enters a dynamic regulation period. During this period, the LS-FET is on until the LS current drops to -2.5A. This discharges the output to keep it within the normal range. If the OV still remains, the LS-FET turns on again after a 400ns delay. The MP2319 exits this regulation period when the feedback voltage is decreased below 106.5% of the reference voltage.

Under-Voltage Lockout (UVLO)

The MP2319 has under-voltage lockout protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MP2319 powers up. The MP2319 shuts off when the input voltage is lower than the UVLO falling threshold voltage. UVLO is a non-latch protection.

Pre-Bias Start-Up

The MP2319 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start capacitor voltage exceeds the sensed output voltage at FB, the part begins working normally.

Output Discharge

The MP2319 has a discharge function that provides an active discharge path for the external output capacitor. The function is active when the part is in the EN off state. When EN is off, the HS-FET turns off, and the LS-FET turns on to discharge V_{OUT}. When the LS-FET current reaches -1A, the LS-FET turns off. After a 400ns delay, the LS-FET turns on again. This behavior repeats until FB low occurs.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. V_{IN} regulates the bootstrap capacitor voltage through D1, M1, R4, C4, L1, and C2 internally (see Figure 5). If V_{IN} - V_{SW} exceeds 5V, U2 regulates M1 to maintain a 5V BST voltage across C4.

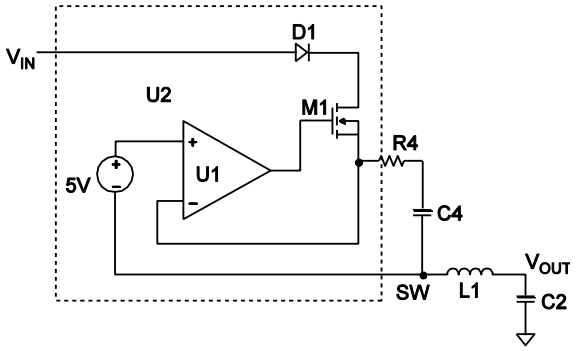


Figure 5: Internal Bootstrap Charger Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path initially to avoid any fault triggering. The COMP voltage (V_{COMP}) and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the Typical Application on page 1). Refer to Table 1 to choose R1. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (2)$$

The feedback circuit is shown in Figure 6.

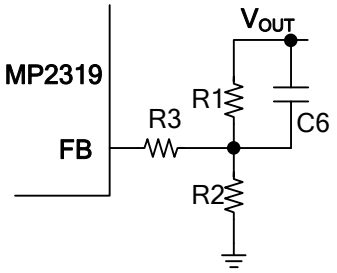


Figure 6: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	C6 (pF)
1	30	120	1	100
1.2	30	60.4	1	100
1.8	30	24	1	100
2.5	30	14	1	100
3.3	30	9.53	1	100
5	30	5.76	1	100

Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. An inductor with a larger value results in less ripple current and a lower output ripple voltage. However, the larger-value inductor also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current. The peak inductor current should be below the maximum switch current limit.

The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, which can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to V_{IN} as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (9)$$

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Besides the output ripple, a larger output capacitor can also achieve a better load transient response. Maximum output capacitor limitations should be considered in design applications, also. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and fails to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (20):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (20)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{ss} is the soft-start time.

PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for proper function and stable operation. Poor layout design can result in poor line or load regulation and stability issues. To achieve better performances, it is recommended to use two-layer boards. Figure 7 shows the top and bottom layers. For best results, refer to Figure 7 and follow the guidelines below.

1) Place the high current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2) Keep the input capacitor as close to IN and GND as possible.
3) Place the external feedback resistors next to FB.
4) Keep the switching node (SW) short and away from the feedback network.

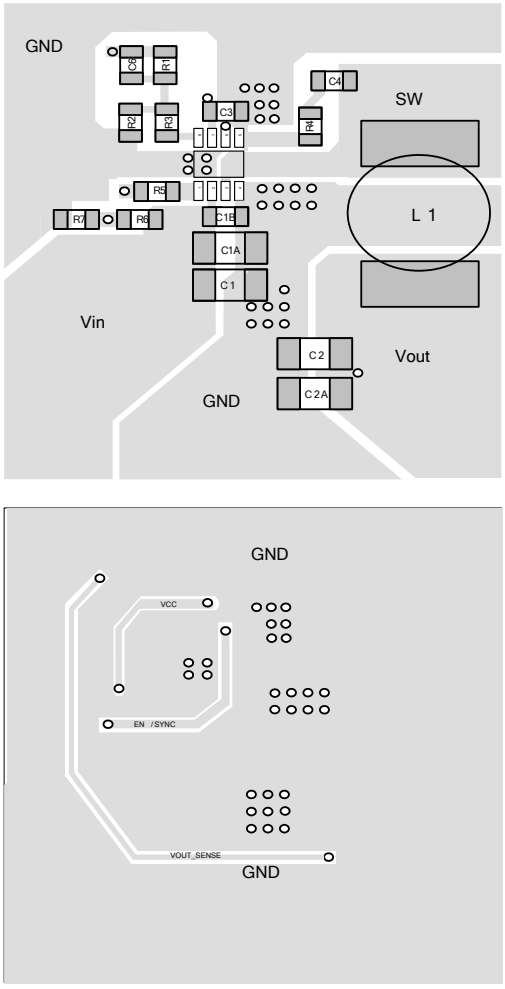


Figure 7: Sample Board Layout

Design Example

Table 2 shows a design example when ceramic capacitors are applied.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	3A

The detailed application schematics are shown in Figure 8 through Figure 13. The typical performance and waveforms are shown in the Typical Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS

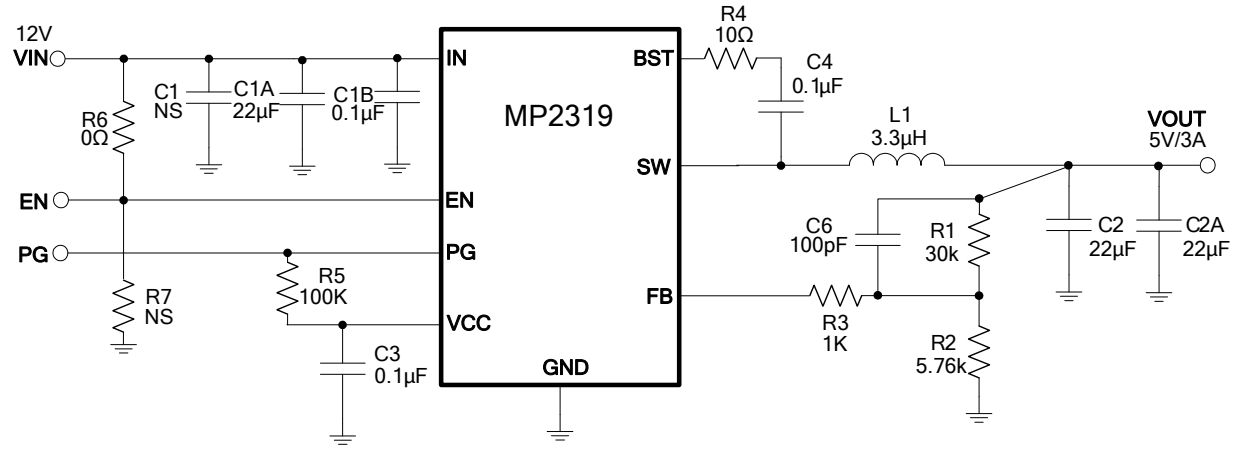


Figure 8: Typical Application Circuit $12V_{IN}$, $5V_{OUT}$/3A

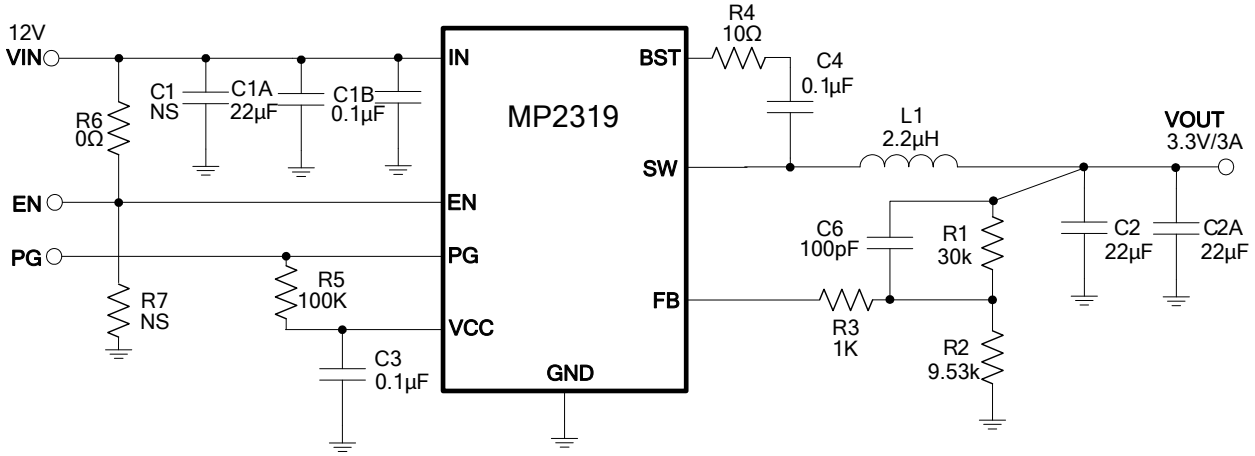


Figure 9: Typical Application Circuit $12V_{IN}$, $3.3V_{OUT}$/3A

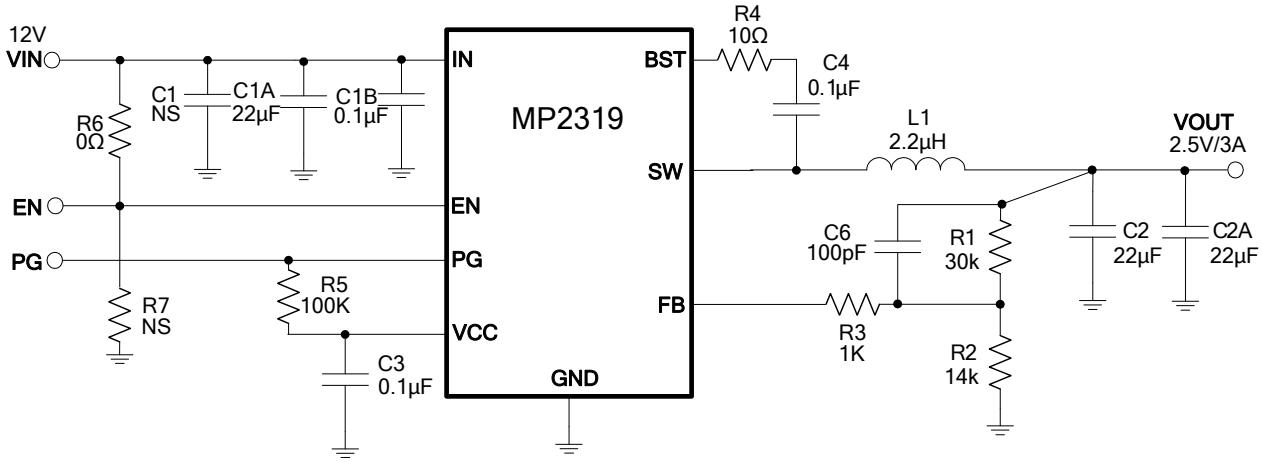


Figure 10: Typical Application Circuit $12V_{IN}$, $2.5V_{OUT}$/3A

TYPICAL APPLICATION CIRCUITS *(continued)*

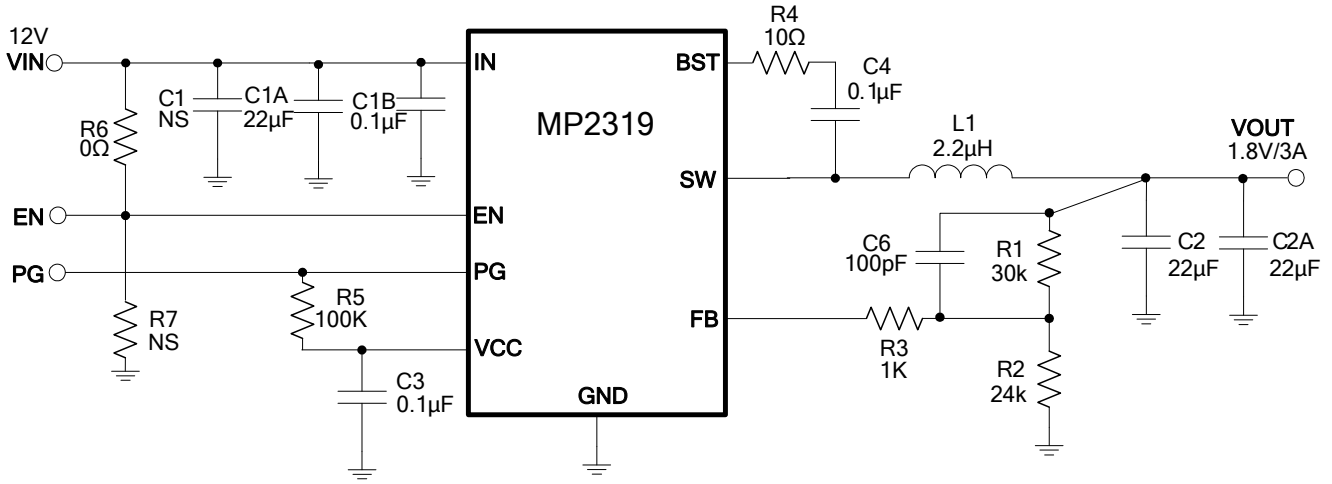


Figure 11: Typical Application Circuit $12V_{IN}$, $1.8V_{OUT}$/3A

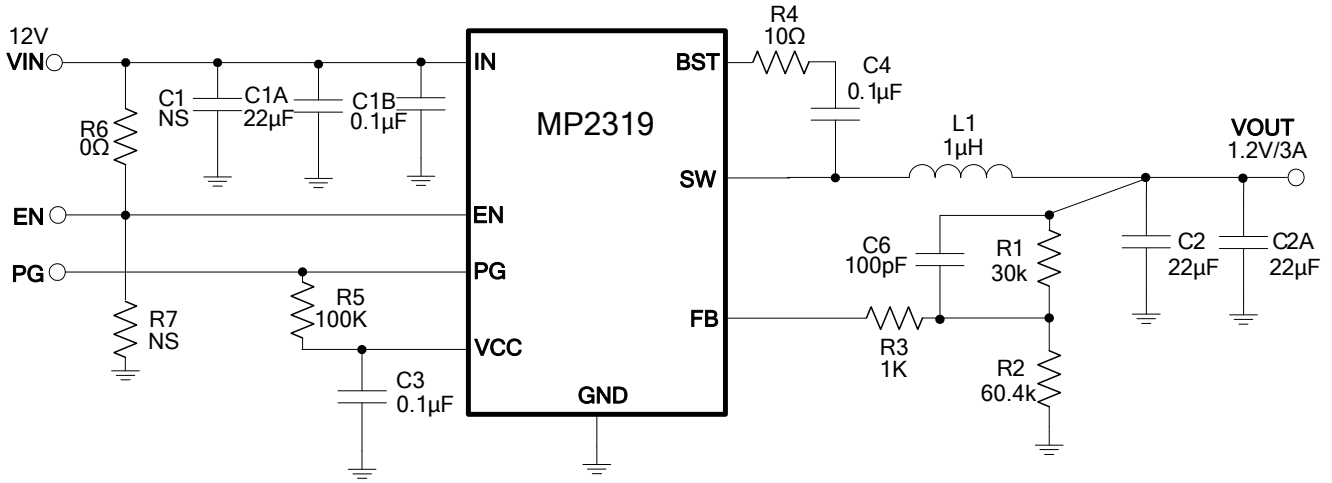


Figure 12: Typical Application Circuit $12V_{IN}$, $1.2V_{OUT}$/3A

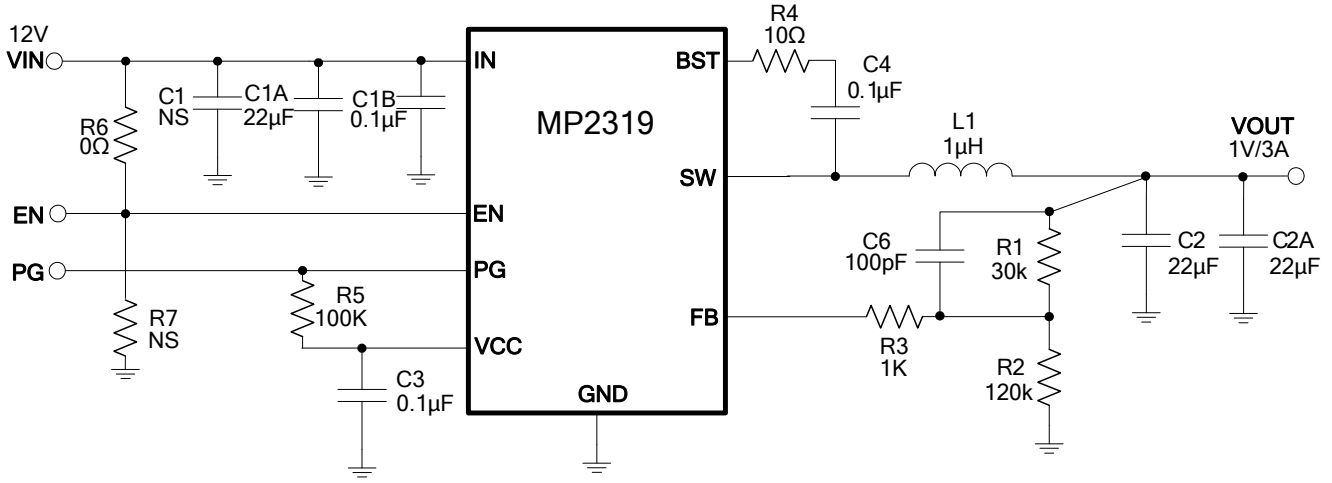
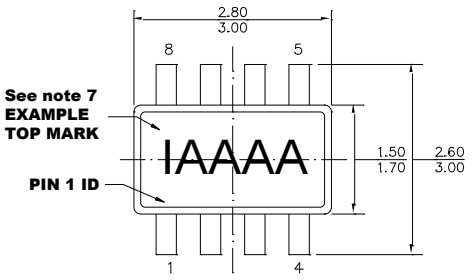


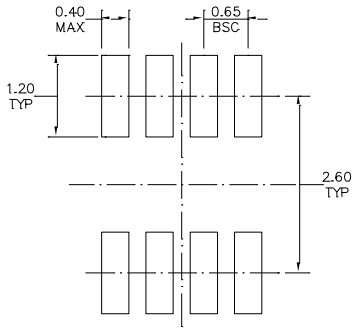
Figure 13: Typical Application Circuit $12V_{IN}$, $1V_{OUT}$/3A

PACKAGE INFORMATION

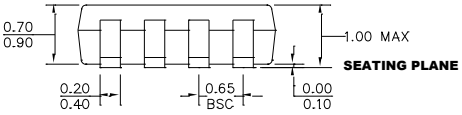
TSOT23-8



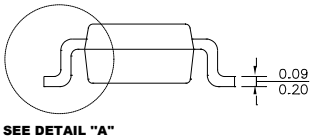
TOP VIEW



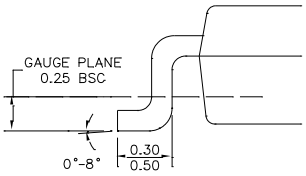
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)