

## DESCRIPTION

The MP6507 is a bipolar stepper-motor driver with dual, built-in full-bridges consisting of N-channel power MOSFETs.

It operates from a supply voltage range of 2.7V to 15V, and can deliver motor current up to 700mA per channel. The internal safety features include sinking and sourcing current limits implemented with external sensors, under-voltage lockout and thermal shutdown. An over-temperature output flag is available to indicate thermal shutdown.

The MP6507 is available in 16-pin, 5.0mm×6.4mm TSSOP-EP and TSSOP, 3mm×3mm and 4mm×4mm QFN package with an exposed thermal pad on the back.

## FEATURES

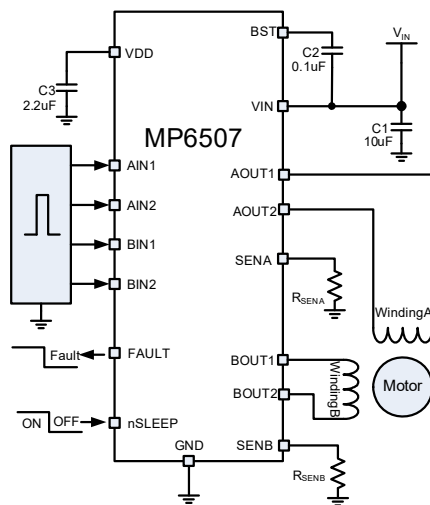
- Wide 2.7V-to-15V Input Voltage Range
- Two Internal Full-Bridge Drivers
- Low MOSFET On Resistance (HS: 500mΩ; LS: 500 mΩ)
- Internal Charge Pump for the High-Side Driver
- Low Quiescent Current: 1.1mA
- Low Sleep Current: 1μA
- Thermal Shutdown and Under-Voltage Lockout Protection
- Over-Temperature Output Flag
- Thermally-Enhanced Surface-Mount Package

## APPLICATIONS

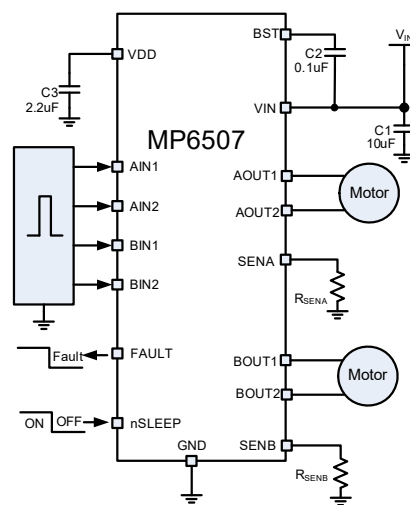
- POS Printers
- Video Security Camera
- Digital Still Cameras
- Battery Powered Toys

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## TYPICAL APPLICATION



Stepper Motor Application



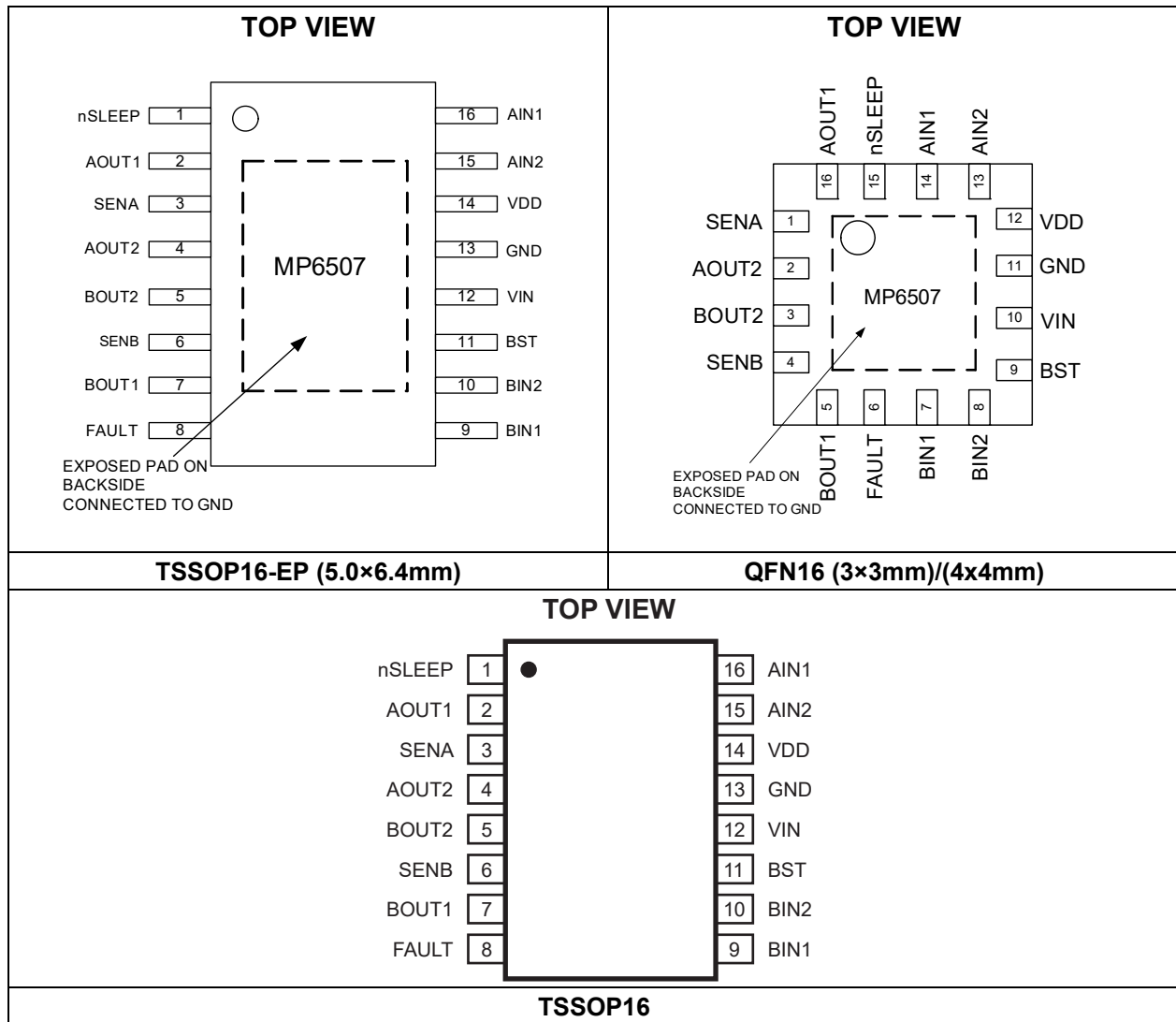
Dual DC Motor Application

## ORDERING INFORMATION

Part Number	Package	Top Marking
MP6507GF*	TSSOP16-EP (5.0×6.4mm)	MP6507
MP6507GQ**	QFN16 (3×3mm)	AEC
MP6507GR***	QFN16 (4×4mm)	MP6507
MP6507GM****	TSSOP16 (5.0×6.4mm)	MP6507

- \* For Tape & Reel, add suffix -Z (e.g. MP6507GF-Z);
- \*\* For Tape & Reel, add suffix -Z (e.g. MP6507GQ-Z);
- \*\*\*For Tape & Reel, add suffix -Z (e.g. MP6507GR-Z);
- \*\*\*\*For Tape & Reel, add suffix -Z (e.g. MP6507GM-Z);

## PACKAGE REFERENCE



**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

Supply Voltage $V_{IN}$ .....	-0.3V to 18V
AOUTx Voltage $V_{AOUTx}$ .....	-0.3V to $V_{IN}+1V$
BOUTx Voltage $V_{BOUTx}$ .....	-0.3V to $V_{IN}+1V$
BST Voltage $V_{BST}$ .....	-0.3V to $V_{IN}+7V$
Sense Voltage $V_{SENx}$ .....	-0.3V to 0.5V
All Other Pins .....	-0.3V to 6.5V
Junction Temperature .....	150°C
Lead Temperature .....	260°C
Continuous Power Dissipation ( $T_A = +25^\circ\text{C}$ ) <sup>(2)</sup>	
QFN16 (3×3mm) .....	2.1W
QFN16 (4×4mm) .....	2.7W
TSSOP16-EP (5.0×6.4mm) .....	2.8W
TSSOP16 .....	1.4W
Operating Temperature .....	-40°C to +85°C

**Recommended Operating Conditions <sup>(3)</sup>**

Supply Voltage $V_{IN}$ .....	2.7V to 15V
Output Current $I_{A/BOUx}$ .....	700mA
Operating Junction Temp. ( $T_J$ ) .....	-40°C to +125°C

<b>Thermal Resistance <sup>(4)</sup></b>	<b><math>\theta_{JA}</math></b>	<b><math>\theta_{JC}</math></b>
QFN16(3×3mm) .....	60 .....	12... °C/W
QFN16(4×4mm) .....	46 .....	10... °C/W
TSSOP16-EP(5.0×6.4mm) .....	45 .....	10... °C/W
TSSOP16 .....	90 .....	30... °C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX)- $T_A$ )/ $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

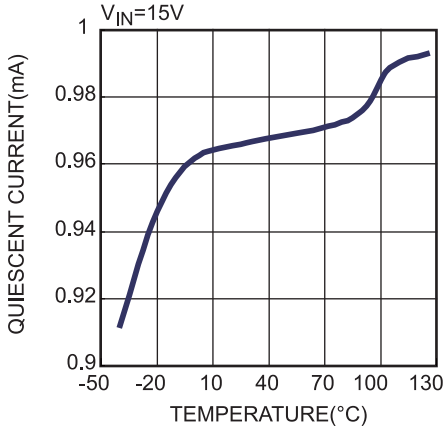
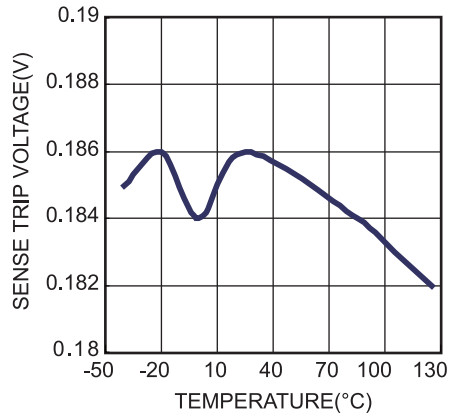
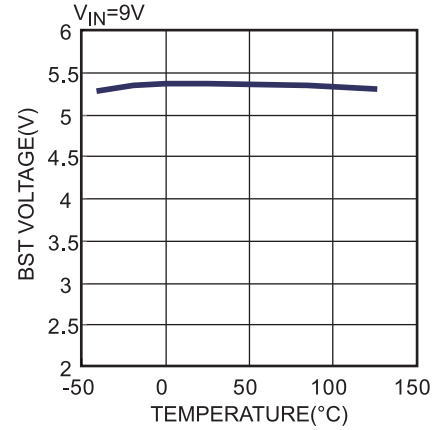
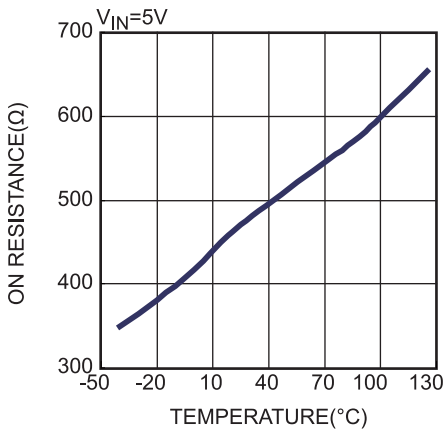
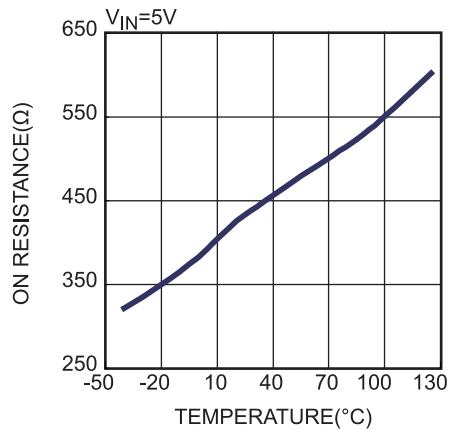
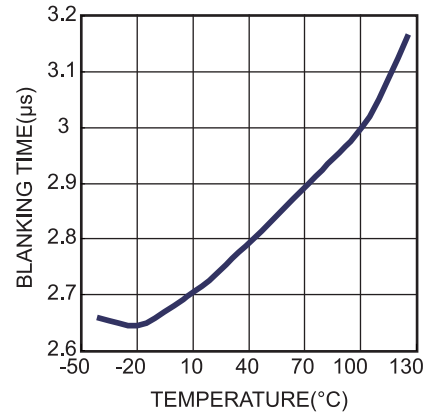
## ELECTRICAL CHARACTERISTICS

$V_{IN} = 2.7V$  to  $15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

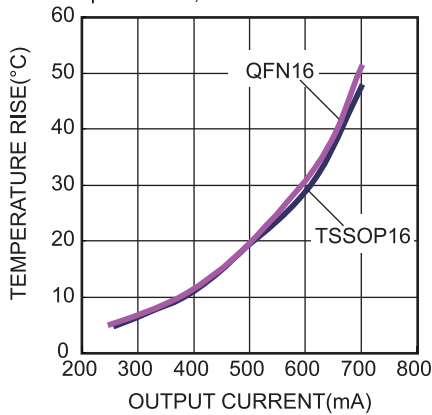
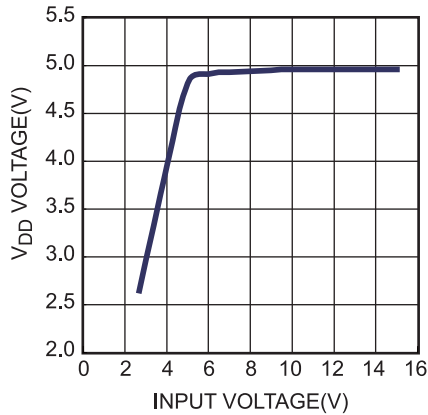
Parameter	Symbol	Condition	Min	Type	Max	Units
<b>Power Supply</b>						
Input Supply Voltage	$V_{IN}$		2.7		15	V
Quiescent Current	$I_{IN}$	nSLEEP=1, $I_{OUT}=0$ , Output disable			1.1	mA
	$I_{IN\_SLEEP}$	nSLEEP=0, $V_{IN}=5V$			1	$\mu A$
<b>Integrated MOSFETs</b>						
Output On Resistance	$R_{HS}$	$I_{OUT}=500mA$ , $V_{IN}=5V$ $T_J=25^\circ C$		460		$m\Omega$
		$I_{OUT}=500mA$ , $V_{IN}=2.7V$ $T_J=25^\circ C$		565	680	$m\Omega$
		$I_{OUT}=500mA$ , $V_{IN}=5V$ $T_J=85^\circ C$		570		$m\Omega$
		$I_{OUT}=500mA$ , $V_{IN}=2.7V$ $T_J=85^\circ C$		700		$m\Omega$
	$R_{LS}$	$I_{OUT}=500mA$ , $V_{IN}=5V$ $T_J=25^\circ C$		395		$m\Omega$
		$I_{OUT}=500mA$ , $V_{IN}=2.7V$ $T_J=25^\circ C$		515	680	$m\Omega$
		$I_{OUT}=500mA$ , $V_{IN}=5V$ $T_J=85^\circ C$		490		$m\Omega$
		$I_{OUT}=500mA$ , $V_{IN}=2.7V$ $T_J=85^\circ C$		650		$m\Omega$
Body-Diode Forward Voltage	$V_F$	$I_{OUT}=500mA$			1	V
<b>Control Logic</b>						
UVLO Threshold (Rising)	$V_{IN\_RISE}$				2.5	V
UVLO Hysteresis	$V_{HYS}$			70		mV
Input Logic 'Low' Threshold	$V_{IL}$				0.6	V
Input Logic 'High' Threshold	$V_{IH}$		2			V
nSLEEP Logic, Low	$V_{SLEEP\_L}$				0.4	V
nSLEEP Logic, High	$V_{SLEEP\_H}$		2			V
Fault Output Logic, Low	$V_{FAULT\_L}$	Flag triggered by OTP 1mA Current.			200	mV
Fault Output Leakage Current	$I_{LEAK\_FAULT}$	$V_{FAULT}=5V$			1	$\mu A$
Constant Off Time	$T_{OFF}$			27		$\mu s$
Propagation Delay Time (On)	$T_{ON\_DELAY}$	INx high to OUTx on 10mA Source Current	50	150	250	ns
Propagation Delay Time (Off)	$T_{OFF\_DELAY}$	INx low to OUTx off	50	150	250	ns

**ELECTRICAL CHARACTERISTICS (continued)**
 **$V_{IN} = 2.7V$  to  $15V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.**

Parameter	Symbol	Condition	Min	Type	Max	Units
Cross Over Delay	$T_{CROSS}$	HS off to LS on or LS off to HS on for one bridge arm	200	425	650	ns
Sleep Mode Wakeup Time	$T_{WAKE}$	Sleep inactive high to full bridge turn on ( $V_{BST}=100nF$ )			1.5	ms
<b>Protection Circuitry</b>						
Current Limit Sense Trip Voltage	$V_{TRIP}$		145	185	225	mV
Blanking Time	$T_{BLANK}$		2.1	2.7	3.3	$\mu s$
Thermal Shutdown				165		$^{\circ}C$
Thermal Shutdown Hysteresis				15		$^{\circ}C$

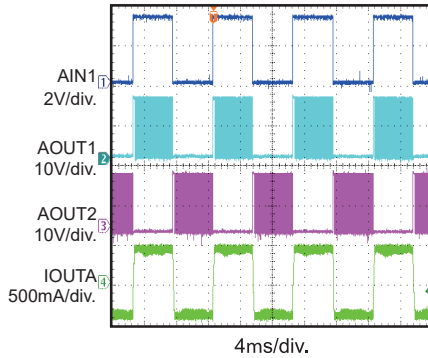
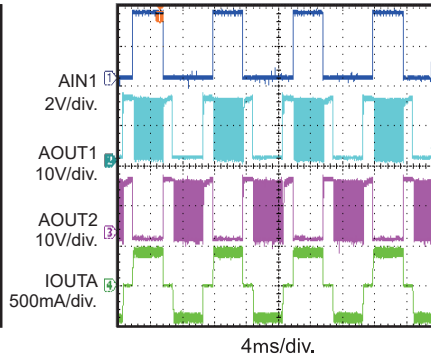
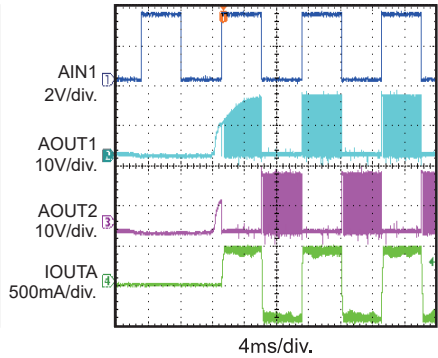
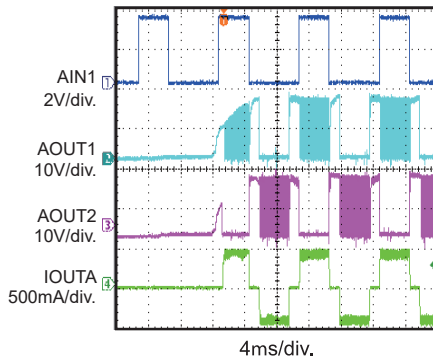
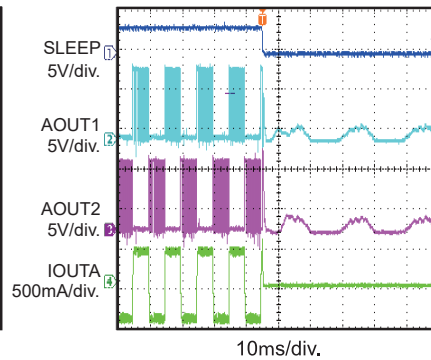
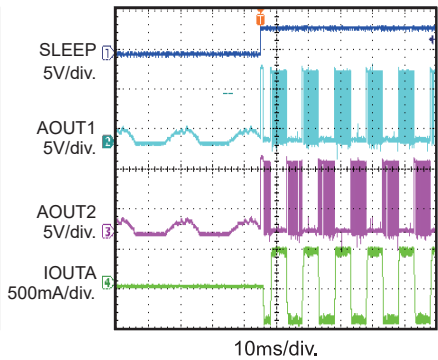
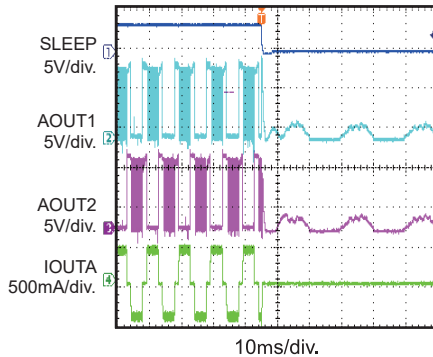
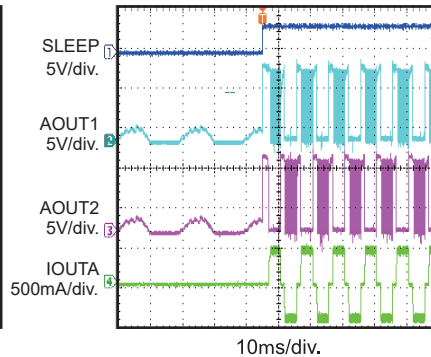
**TYPICAL CHARACTERISTICS**
**Quiescent Current vs. Temperature**

**Sense Trip Voltage vs. Temperature**

**BST Voltage vs. Temperature**

**Bridge A HS ON RESISTANCE vs. Temperature**

**Bridge B HS ON RESISTANCE vs. Temperature**

**Blanking Time vs. Temperature**

**Temperature Rise vs. Output Current**

V<sub>IN</sub>=9V, Full Step(100Hz), T<sub>A</sub>=25°C, Open Frame, test based on EVB


**V<sub>DD</sub> Voltage vs. Input Voltage**


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Performance waveforms are tested on the evaluation board of the Design Example section.  
 $I_{OUT}=500mA$ ,  $F_{STEP}=100Hz$ , Stepper Motor:  $L=2mH$ ,  $R=10\Omega$ ,  $T_A=25^\circ C$ , unless otherwise noted.

**Steady State-Full Step**  
 $V_{IN}=15V$ 

**Steady State-Half Step**  
 $V_{IN}=15V$ 

**Power Ramp Up-Full Step**  
 $V_{IN}=15V$ 

**Power Ramp Up-Half Step**  
 $V_{IN}=15V$ 

**Sleep Entry-Full Step**  
 $V_{IN}=9V$ 

**Sleep Recovery-Full Step**  
 $V_{IN}=9V$ 

**Sleep Entry-Half Step**  
 $V_{IN}=9V$ 

**Sleep Recovery-Half Step**  
 $V_{IN}=9V$ 


## PIN FUNCTIONS

QFN16 Pin #	TSSOP16 Pin #	Name	Description
1	3	SENA	Channel A Sense. Connect to current sensor resistor for channel A.
2	4	AOUT2	Connect to motor winding A.
3	5	BOUT2	Connect to motor winding B.
4	6	SENB	Channel B Sense. Connect to current sensor resistor for channel B.
5	7	BOUT1	Connect to motor winding B.
6	8	FAULT	Logic low when in over-temperature fault condition.
7	9	BIN1	Gate signal input to control BOUT1.
8	10	BIN2	Gate signal input to control BOUT2.
9	11	BST	Charge Pump Output. Connect a 10nF-to-100nF ceramic capacitor to VIN
10	12	VIN	Power Supply Input. Ranges from 2.7V to 15V.
11	13	GND	Ground
12	14	VDD	Internal control and logic supply voltage. Connect a 2.2uF capacitor from VDD to GND. VDD is for internal use only. Do not connect any external load to VDD pin.
13	15	AIN2	Gate signal input to control AOUT2.
14	16	AIN1	Gate signal input to control AOUT1.
15	1	nSLEEP	Sleep Logic Input. Logic low for sleep mode and logic high to enable the device
16	2	AOUT1	Connect to motor winding A



## BLOCK DIAGRAM

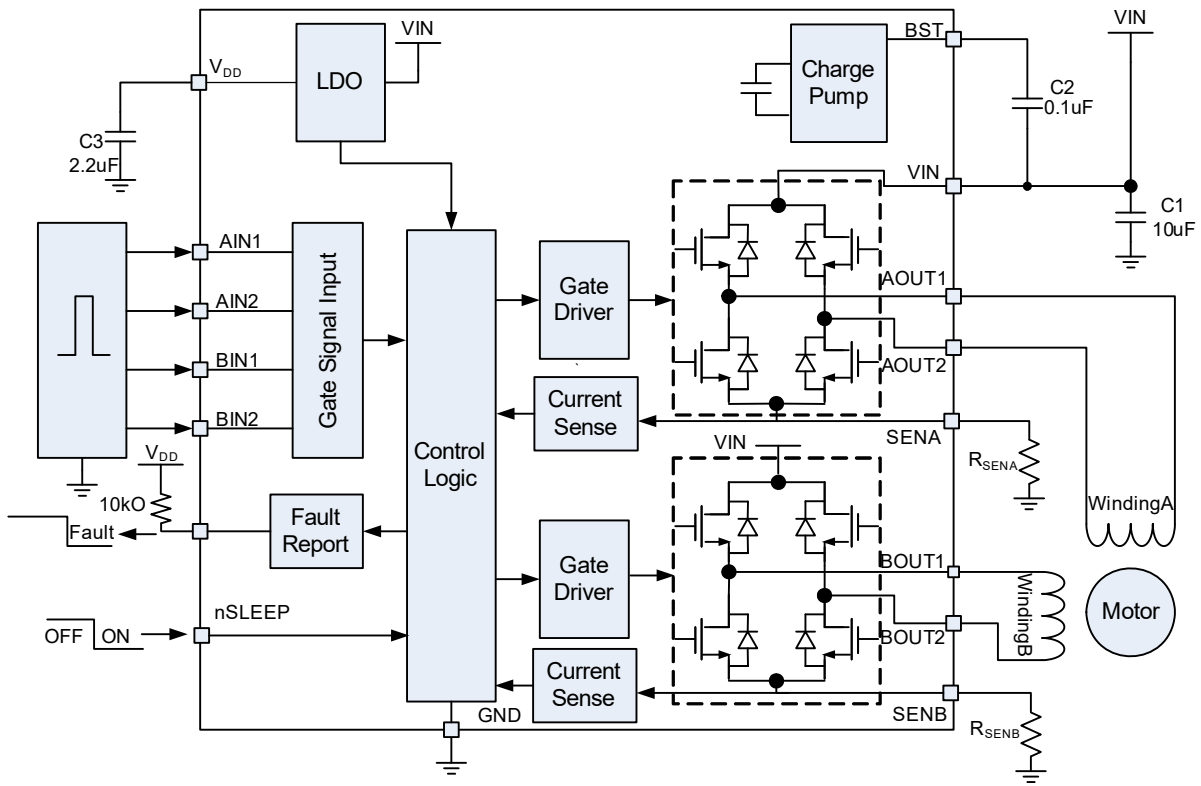


Figure 1: Function Block Diagram

## OPERATION

The MP6507 is a motor driver that integrates 8 N-channel power MOSFETs for dual, internal full-bridges with 700mA output current capability over an input voltage range of 2.7V to 15V. It can drive a stepper motor or two DC motors.

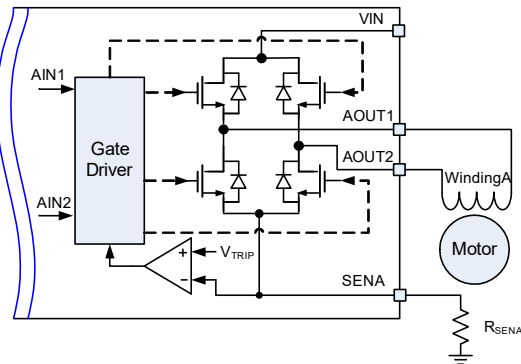
The motor output current can be either controlled by an external pulse width modulator (PWM) or internal PWM current controller.

The MP6507 includes the following fault protections: under-voltage lockout (UVLO) and over-temperature protection (OTP).

It also provides a low-power sleep mode.

### External PWM Current Control

The motor current can be regulated by applying external PWM signals on the input pins AIN1, AIN2, BIN1 and BIN2. For phase A, the AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2; similarly for phase B, these BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2.



**Figure 2: Full-Bridge Control Circuit**

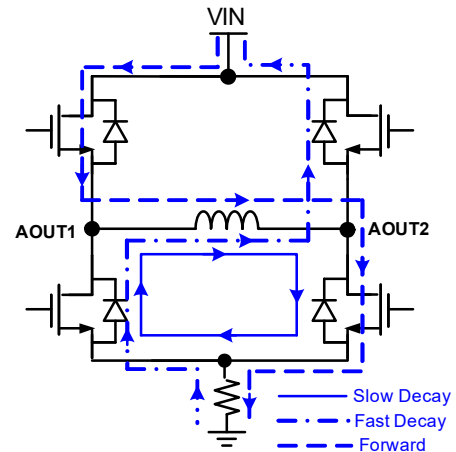
Table 1 shows the input signal logic and bridge output state.

**Table 1: Full-Bridge Gate Logic**

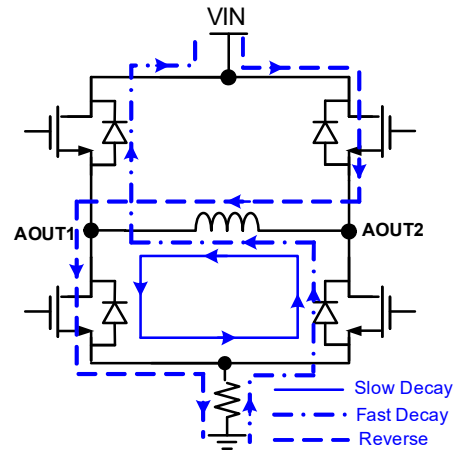
A/BIN1	A/BIN2	A/BOUT1	A/BOUT2
L	L	High Impedance	High Impedance
L	H	GND	VIN
H	L	VIN	GND
H	H	GND	GND

In external PWM control mode, the winding's inductive current ramps up when the high-side MOSFET is on and freewheels during the high-side MOSFET's off time to cause the recirculation current.

There are two modes for this recirculation current: slow decay and fast decay, both of which are shown in Figure 3 for forward operation and Figure 4 for reverse operation.



**Figure 3: Forward Operation**



**Figure 4: Reverse Operation**

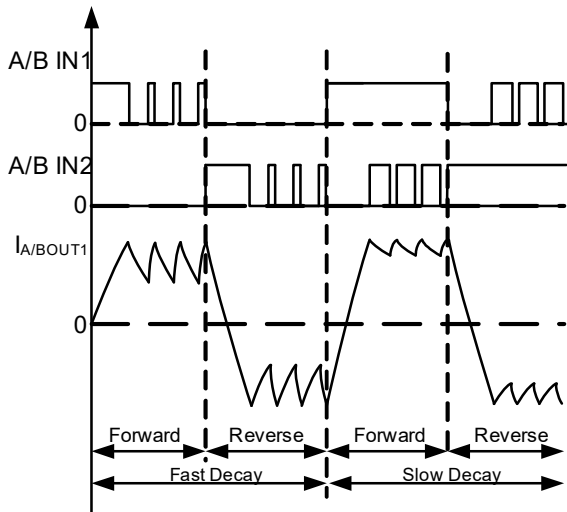
For slow decay mode, the current circulates through the two low-side MOSFETs. For fast decay mode, the current flows through the body diodes of the other diagonal two MOSFETS.

To configure the MP6507 for fast decay mode, apply the PWM signal to one input pin and keep

the other input pin low; for slow decay mode, apply the PWM signal to one input pin and keep the other input pin high. See Table 2 for more configuration details and Figure 5 for detailed waveforms.

**Table 2: PWM Control**

A/BIN1	A/BIN2	Mode
H (PWM)	L	Forward
L (PWM)	L	Fast Decay
L	H (PWM)	Reverse
L	L (PWM)	Fast Decay
H	L (PWM)	Forward
H	H (PWM)	Slow Decay
L (PWM)	H	Reverse
H (PWM)	H	Slow Decay


**Figure 5: External PWM Current Control Waveform**  
**Internal PWM Current Control**

For this control method, the motor current is regulated by an internal constant off-time PWM current control circuit as the following:

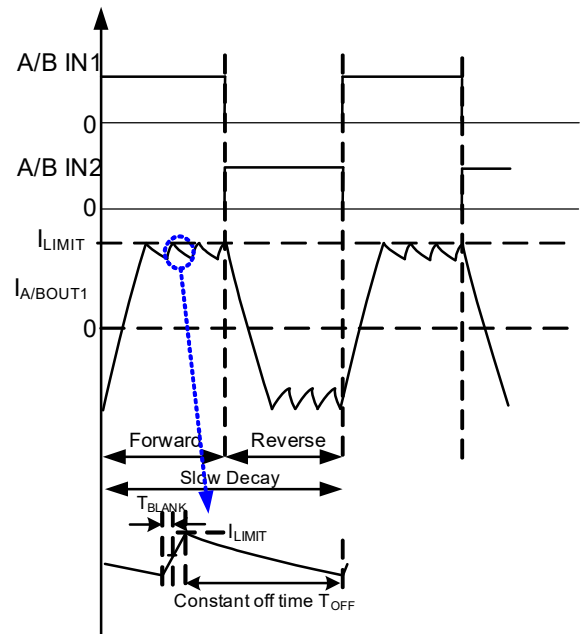
- Initially, a diagonal pair of MOSFETs turns on so current can flow through the motor winding.
- The current increases in the motor winding, which is sensed by an external sense resistor ( $R_{SENSE}$ ). During the initial blanking time  $T_{BLANK}$  (3 $\mu$ s), the high-side MOSFET always turns on in spite of current limit detection.
- When the voltage across  $R_{SENSE}$  reaches the internal reference voltage threshold  $V_{TRIP}$  (185mV), the internal current

comparator shuts off the high-side MOSFET.

- The stepper motor's inductance causes the current to freewheel through the two low-side MOSFETs (slow decay).
- During this freewheeling time, the current decreases until the internal clock reaches its' constant off time (typically 27 $\mu$ s). After that, the high-side MOSFET is enabled to increase the winding current again.
- The cycle then repeats.

Calculate the current limit as:

$$I_{LIMIT} = \frac{V_{TRIP}}{R_{SENSE}} \quad (1)$$


**Figure 6: Internal PWM Current Control Waveform**  
**Sleep Mode**

The MP6507 provides low-power standby sleep mode.

Connect the nSLEEP pin to logic low to enable a low-power sleep state. In this state, the two full bridges are disabled and the internal circuits such as the gate drive, internal regulator, and charge pump all shut down. Connect the nSLEEP pin to logic high to wake up the MP6507

from sleep mode, though there is a delay time of ~1ms until the internal circuitry stabilizes.

### Blanking Time

There is usually a current spike during the switching transition due to the body diode's reverse-recovery current or the distributed inductance or capacitance. This current spike requires filtering to prevent it from erroneously shutting down the high-side MOSFET. An internal blanking time  $T_{BLANK}$  blanks the output of the current sense comparator when the outputs are switched, which is also the minimum on time for high-side MOSFET.

### Enable

If all the inputs (AIN1, AIN2, BIN1 and BIN2) are logic low, the MP6507's outputs are disabled while the charger pump and internal regulator remain active.

### Synchronous Rectifier

The MP6507 enters a synchronous rectifier (SR) mode during the constant off-time period when

the current limit threshold is exceeded, and the load current freewheels in slow decay SR mode. In slow decay mode, the current freewheels through one low-side MOSFET and the body diode of the other low-side MOSFET to short the winding. The SR mode enables both two low-side MOSFETs, which feature a lower voltage drop and lower power dissipation during decay operation.

### Thermal Shutdown

The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 165°C), the converter is shut down (the fault pin goes low) and recovers once the junction temperature drops to about 150°C (15°C hysteresis).

### UVLO protection

The MP6507 has UVLO protection. When the VIN exceeds the UVLO rising threshold, the MP6507 powers up. It shuts off when VIN drops below the UVLO falling threshold.

## APPLICATION INFORMATION

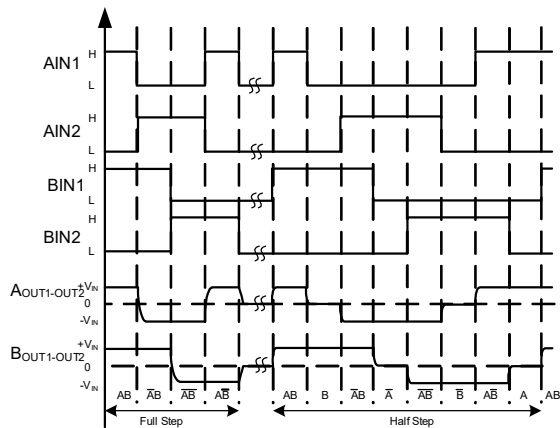
### Driver Mode:

The MP6507 could be configured for both full-step and half-step modes by sequentially energizing the two windings.

Full-step drive energizes two winding phases at any given time. The stator windings are energized as per the sequence shown in Table 3. There are a total of four steps for one cycle in the sequence <sup>(5)</sup>:  $AB \rightarrow \overline{AB} \rightarrow \overline{A}B \rightarrow A\overline{B}$ .

Half-step energizes the stator windings as per the sequence shown in Table 4. There are a total of 8 steps for one cycle:  $AB \rightarrow B \rightarrow \overline{AB} \rightarrow \overline{A} \rightarrow A\overline{B} \rightarrow \overline{B} \rightarrow \overline{AB} \rightarrow A$ .

Figure 7 shows the operating waveforms for both full and half step drives.



**Figure 7: Signal Logic Sequences for Full-Step and Half-Step**

**Table 3 <sup>(6)</sup>: Full-Step Drive Sequence**

Sequence (Full Step)	1	2	3	4
A	+			+
B	+	+		
$\overline{A}$		+	+	
$\overline{B}$			+	+

**Table 4 <sup>(6)</sup>: Half-Step Drive Sequence**

Sequence (Half Step)	1	2	3	4	5	6	7	8
A	+						+	+
B	+	+	+					
$\overline{A}$			+	+	+			
$\overline{B}$					+	+	+	

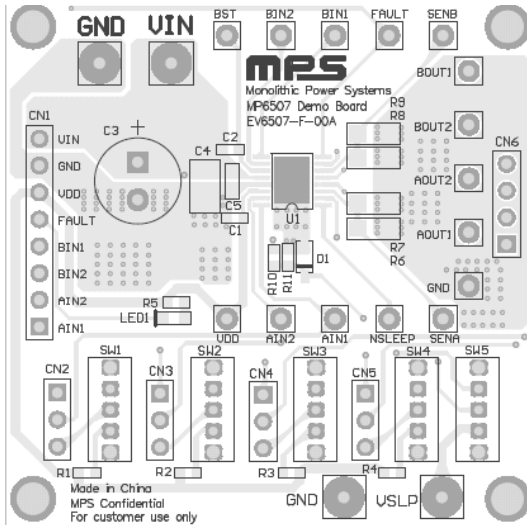
### Note:

- 5) A means +VIN between AOUT1 and AOUT2 for winding A, while  $\overline{A}$  means -VIN between AOUT1 and AOUT2. The same applies to winding B.
- 6) "+" item is the selected winding voltage.

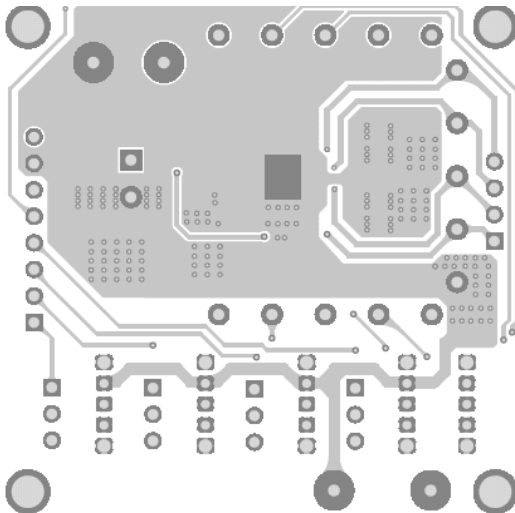
### PCB Layout Guide

The printed circuit board (PCB) should use a heavy ground-plane. The MP6507 must be soldered directly onto the board for better electrical and thermal performance. The sense resistors should be placed as close as possible to the part for accurate current detection.

The MP6507 uses an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to copper on the PCB. Thermal vias are often used to transfer heat to other layers of the PCB.



Top Layer



Bottom Layer

Figure 8: PCB Layout (TSSOP16-EP)

### Design Example

Below is a design example following the application guidelines for the specifications:

Table 5: Design Example

$V_{IN}$	2.7V-15V
$I_{OUT}$	500mA

The detailed application schematic is shown in Figure 9. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.

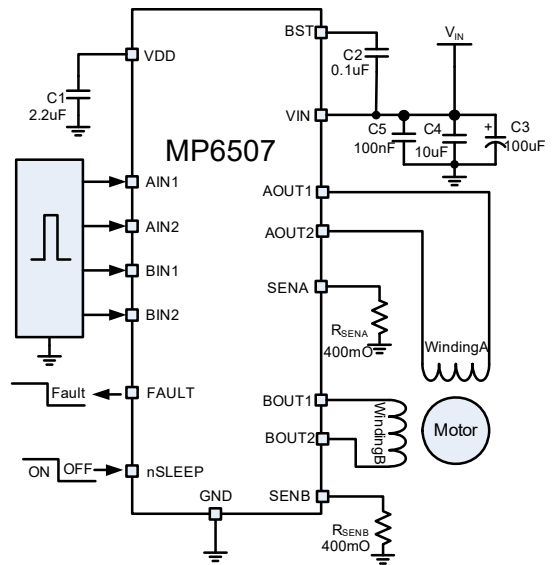
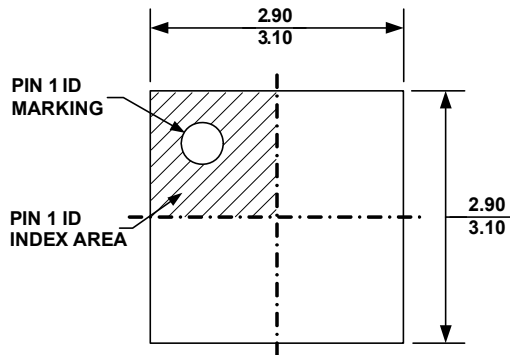


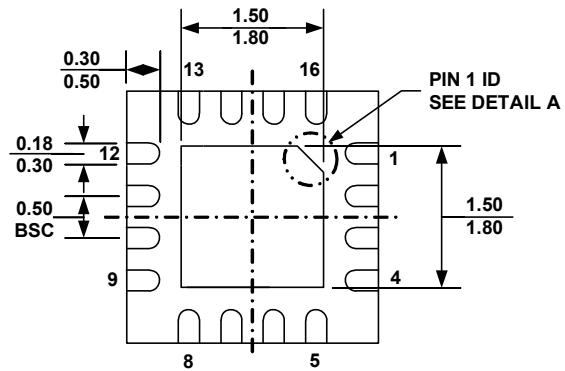
Figure 9: Detailed Application Schematic

# PACKAGE INFORMATION

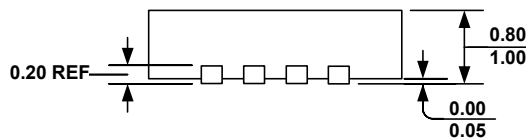
## QFN 16 (3×3mm)



**TOP VIEW**



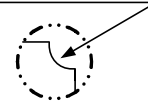
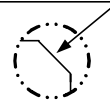
**BOTTOM VIEW**



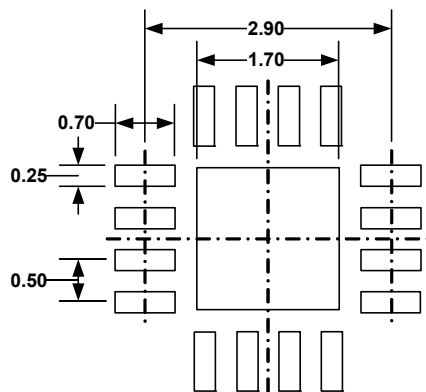
**SIDE VIEW**

**PIN 1 ID OPTION A**  
0.30x45° TYP.

**PIN 1 ID OPTION B**  
R0.20 TYP.



**DETAIL A**

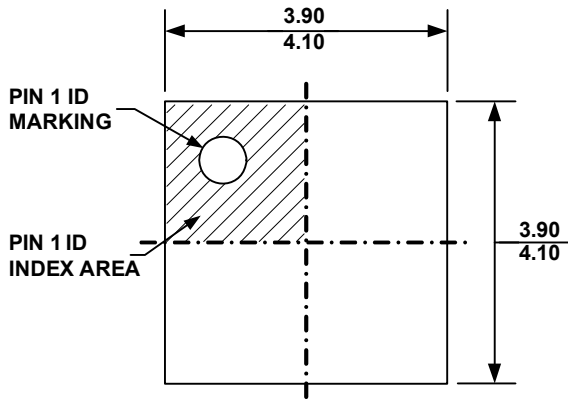


**RECOMMENDED LAND PATTERN**

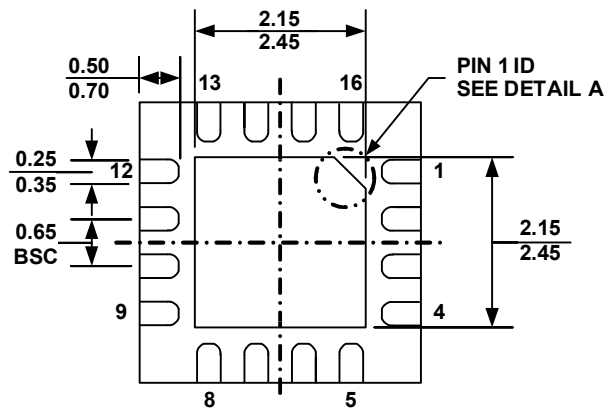
**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX
- 4) DRAWING CONFORMS TO JEDEC MO220, VARIATION VEED-4.
- 5) DRAWING IS NOT TO SCALE

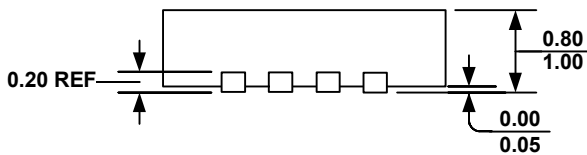
QFN 16 (4×4mm)



TOP VIEW



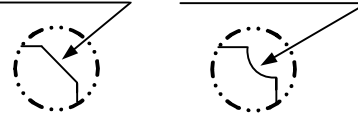
BOTTOM VIEW



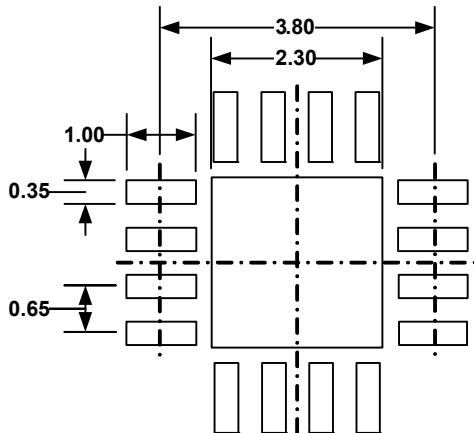
SIDE VIEW

PIN 1 ID OPTION A  
0.45x45° TYP.

PIN 1 ID OPTION B  
R0.25 TYP.



DETAIL A

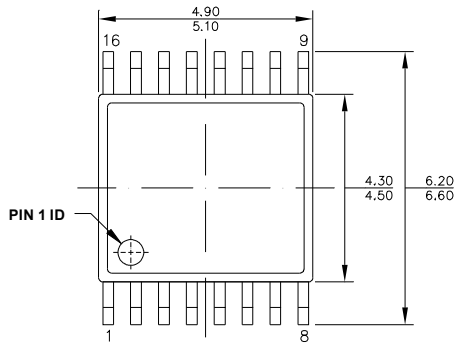
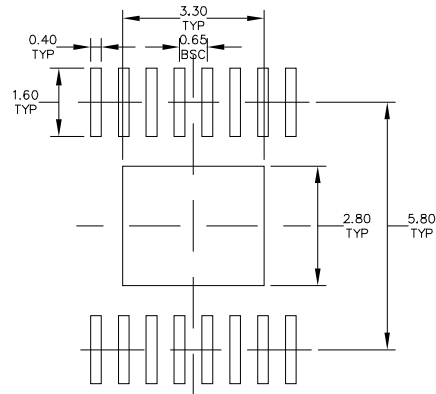
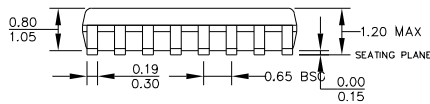
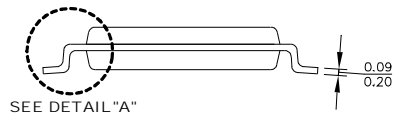
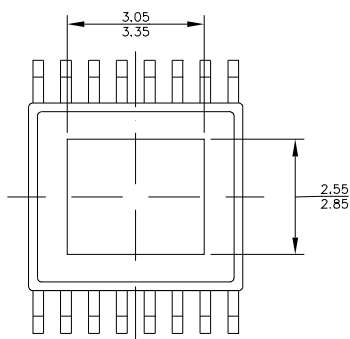
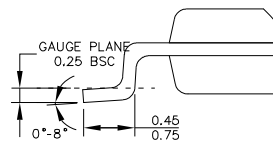


RECOMMENDED LAND PATTERN

NOTE:

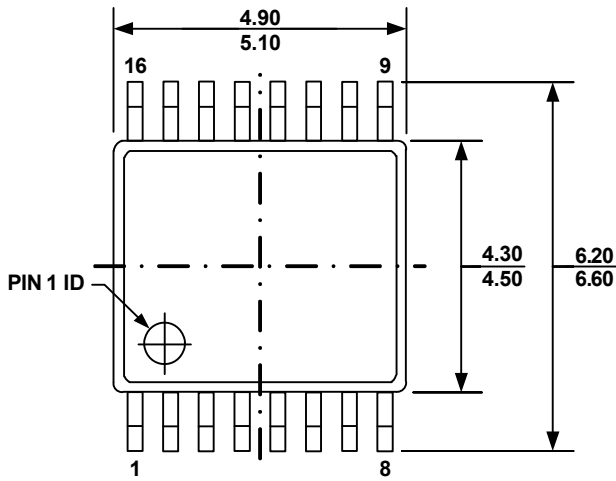
- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX
- 4) JEDEC REFERENCE IS MO-220, VARIATION VGGC.
- 5) DRAWING IS NOT TO SCALE



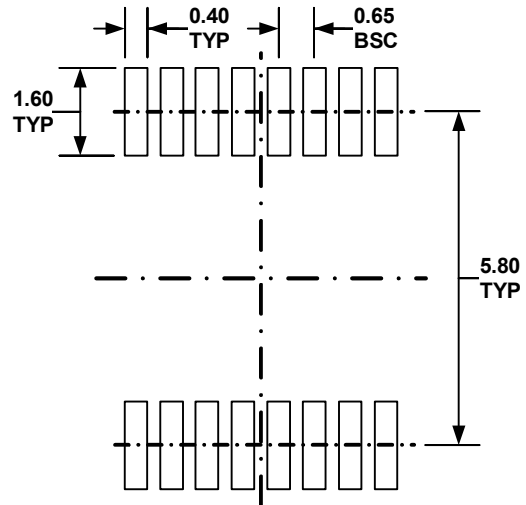
**PACKAGE INFORMATION**
**TSSOP16-EP (5.0×6.4mm)**

**TOP VIEW**

**RECOMMENDED LAND PATTERN**

**FRONT VIEW**

**SIDE VIEW**

**BOTTOM VIEW**

**DETAIL "A"**
**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
- 5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
- 6) DRAWING IS NOT TO SCALE

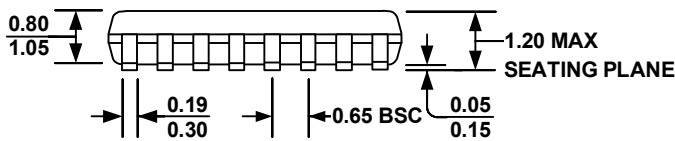
TSSOP16



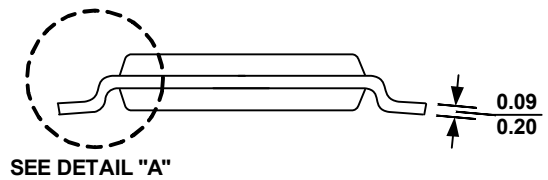
TOP VIEW



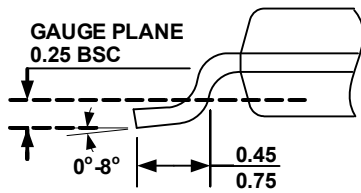
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AB.
- 6) DRAWING IS NOT TO SCALE.

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