MP8714

High-Efficiency, 10A, 17V, Synchronous, Step-Down Converter With External Soft Start and Power Good

The Future of Analog IC Technology

DESCRIPTION

The MP8714 is a high-frequency, synchronous, rectified, step-down, switch-mode converter. This fully integrated solution achieves 10A of output current with excellent load and line regulation over a wide input supply range.

Current mode operation provides fast transient response and eases loop stabilization. EN/SYNC supports external clock synchronization, and an open-drain power good pin (PG) indicates when the output voltage is in the nominal range.

Full protection features include over-voltage protection (OVP), hiccup over-current protection (OCP), and thermal shutdown.

The MP8714 requires a minimal number of readily available, standard, external components and is available in a QFN-14 (3mmx4mm) package.

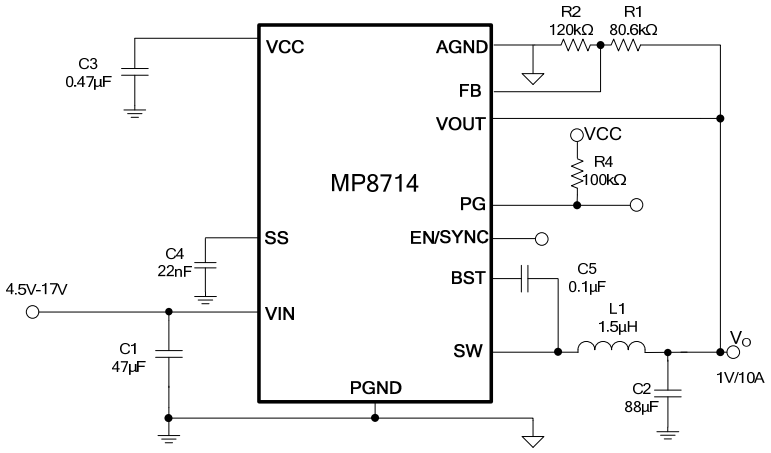
FEATURES

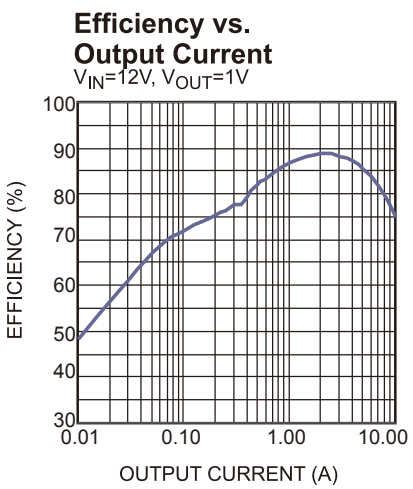
- Wide 4.5V to 17V Operating Input Range
- 10A Continuous Output Current
- 26mΩ High-Side, 11mΩ Low-Side $R_{DS(ON)}$ for Internal Power MOSFETs
- 200kHz - 2MHz Synchronized External Clock
- Programmable Soft-Start (SS) Time
- Open-Drain Power Good (PG) Indicator
- Output Over-Voltage Protection (OVP)
- Thermal Shutdown
- Available in a Small QFN-14 (3mmx4mm) Package

APPLICATIONS

- Flat-Panel Televisions and Monitors
- Set-Top Boxes
- Distributed Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8714GLE	QFN-14 (3mmx4mm)	*See Below*

For Tape & Reel, add suffix –Z (e.g. MP8714GLE–Z)

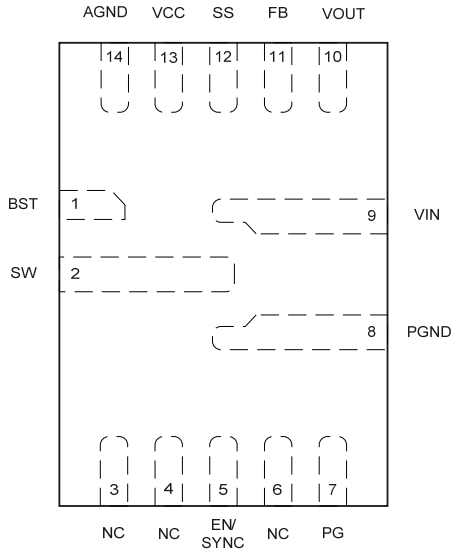
TOP MARKING

MPYW
8714
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
8714: First four digits of the part number
LLL: Lot number
E: Product code

PACKAGE REFERENCE

TOP VIEW



QFN-14 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

VIN ..... -0.3V to 19V
V_{SW} ..... -0.6V (-6V for <10ns) to 20V (24V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
All other pins ..... -0.3V to 5.5V (2)
Continuous power dissipation (T_A = +25°C) (3)
QFN-14 (3mmx4mm) 2.6W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (VIN) ..... 4.5V to 17V
Output voltage (VOUT) ..... 0.6V to VIN x D_{MAX} or 5.5V (5)
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (6)

	θ_{JA}	θ_{JC}	
QFN-14 (3mmx4mm)	48	11	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details of EN/SYNC's ABS MAX rating, please refer to the Enable/SYNC Control section on page 13.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) The output voltage cannot exceed the 5.5V absolute maximum value at any input condition.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to 125°C [7], unless otherwise noted. Typical value is based on the average value when T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		9	13	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, no switching		560	800	μA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 5V		26		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC} = 5V		11		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V or 0V, T_J = 25°C			1	μA
High-side current limit [8]	I_{LIMIT_H}	Under 40% duty cycle	11.7	14		A
Oscillator frequency	f_{SW}	T_J = 25°C	400	500	570	kHz
		T_J = -40°C to 125°C	350		600	
Foldback frequency	f_{VOUT}	V_{FB} = 150mV		0.5		f_{SW}
SYNC frequency range	f_{SYNC}		200		2000	kHz
Maximum duty cycle	D_{MAX}	V_{FB} = 500mV, f_S = 500kHz	93	95		%
Minimum on time [8]	t_{ON_MIN}			40		ns
FB voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to 85°C [8]	588		612	
FB current	I_{FB}	V_{FB} = 620mV		10	50	nA
EN/SYNC pull-up current	I_{EN_PU}	V_{EN} = 0V, T_J = 25°C	4.3	6.2	7.5	μA
		V_{EN} = 0V, T_J = -40°C to 125°C	3.2		8	
EN/SYNC rising threshold	V_{EN_Rise}	T_J = 25°C	1.27	1.38	1.48	V
		T_J = -40°C to 125°C	1.25		1.5	
EN/SYNC hysteresis	V_{EN_HYS}	T_J = 25°C	100	150	200	mV
		T_J = -40°C to 125°C	80		220	
EN/SYNC turn-off delay	EN_{td-off}			10		μs
VIN under-voltage lockout threshold rising	$INUV_{Vth}$	T_J = 25°C	4.03	4.16	4.29	V
		T_J = -40°C to 125°C	4		4.32	
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$		510	610	700	mV
Power good UV threshold rising	PGVth-Hi	T_J = 25°C	0.85	0.9	0.94	VOUT
		T_J = -40°C to 125°C	0.84		0.95	
Power good UV threshold falling	PGVth-Lo	T_J = 25°C	0.64	0.7	0.73	VOUT
		T_J = -40°C to 125°C	0.63		0.74	
Power good deglitch time	PGTd			100	160	μs

ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 12V, T_J = -40°C to 125°C [7], unless otherwise noted. Typical value is based on average value when T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
OVP discharge resistor	R_{OV}	From VOUT to GND		35	70	Ω
OVP rising threshold	V_{EN_Rise}	FB pin, T_J = 25°C	114%	120%	126%	V_{REF}
		FB pin, T_J = -40°C to 125°C	113%		127%	
OVP falling threshold	$V_{EN\ Fall}$	FB pin	101%	105%	108%	V_{REF}
Soft-start current	i_{SS}		7	10	12	μA
VCC voltage	V_{CC}	T_J = -40°C to 125°C	4.75	4.95	5.1	V
VCC load regulation		I_{CC} = 5mA		1	3	%
Thermal shutdown [8]	T_{TSD}			160		°C
Thermal hysteresis [8]	$T_{TSD\ HYS}$			20		°C

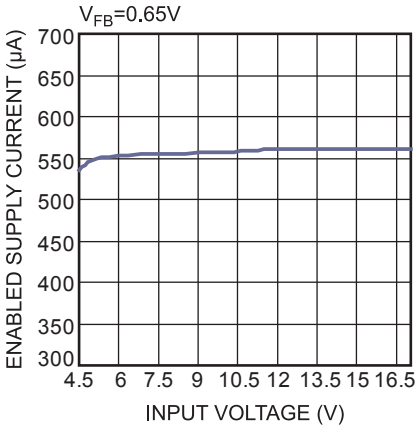
NOTES:

7) Not tested in production, guaranteed by over-temperature correlation.
8) Guaranteed by design and characterization test.

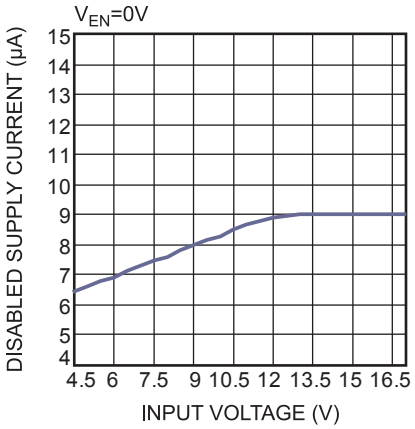
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 12V, VOUT = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

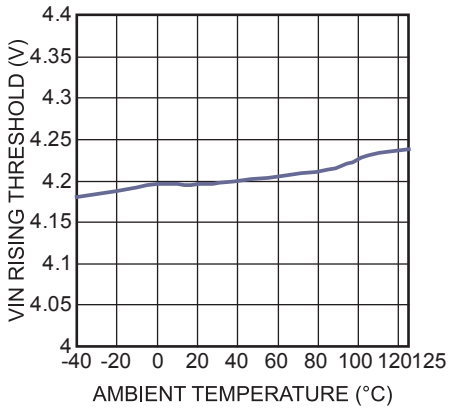
Enabled Supply Current vs. Input Voltage



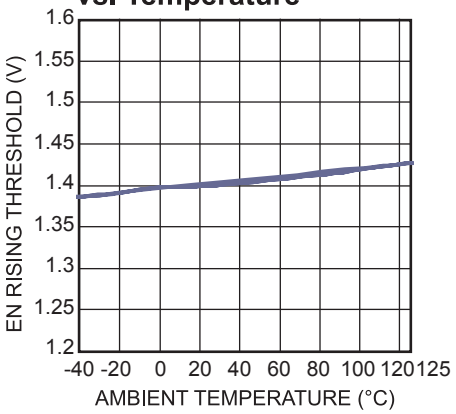
Disabled Supply Current vs. Input Voltage



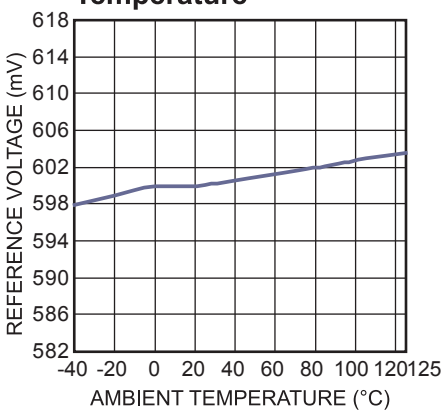
VIN UVLO Rising Threshold vs. Temperature



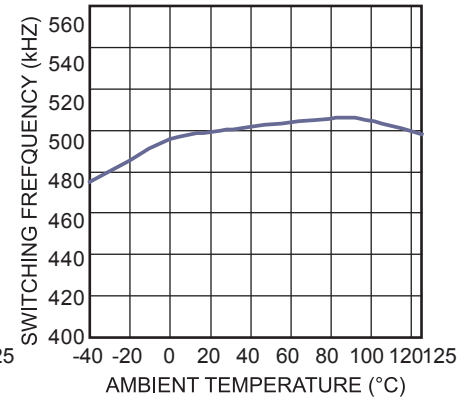
EN/SYNC Rising Threshold vs. Temperature



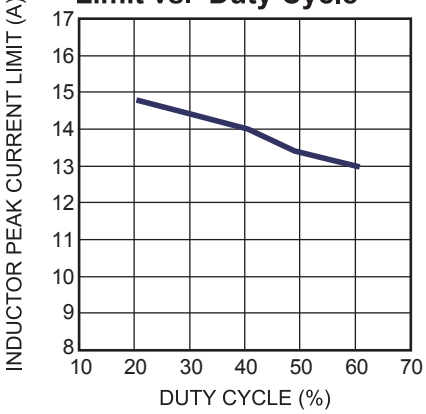
Reference Voltage vs. Temperature



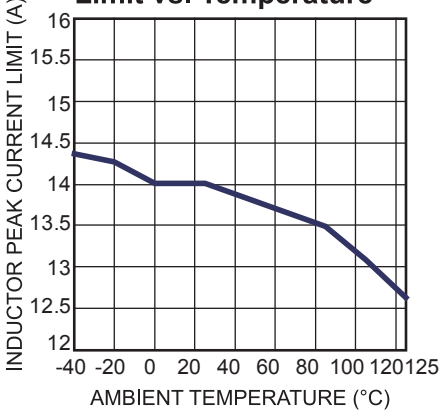
Switching Frequency vs. Ambient Temperature



Inductor Peak Current Limit vs. Duty Cycle



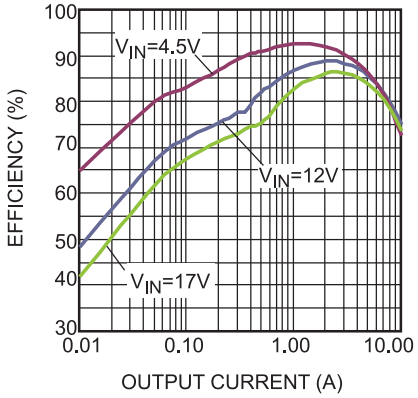
Inductor Peak Current Limit vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

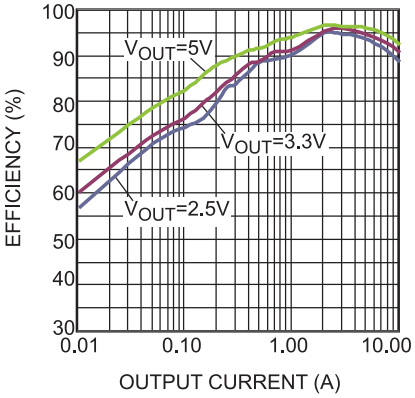
VIN = 12V, VOUT = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Output Current

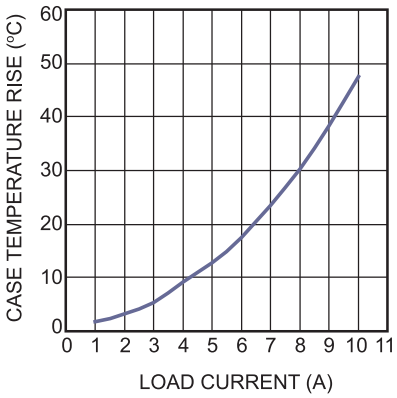


Efficiency vs. Output Current

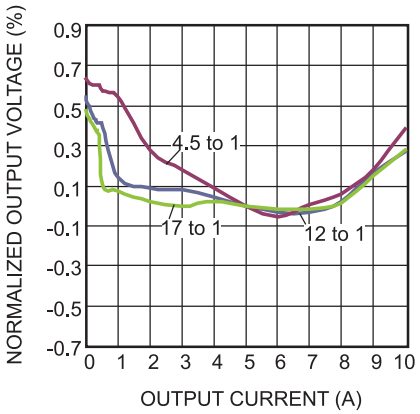
V_{IN}=12V



Case Temperature Rise vs. I_{OUT}

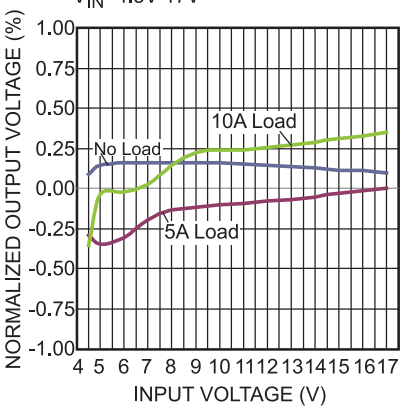


Load Regulation



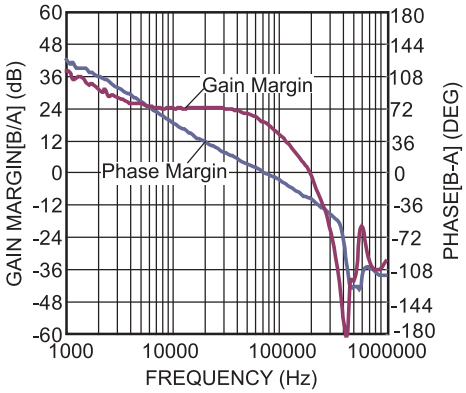
Line Regulation

V_{IN}=4.5V-17V



Bode Plot

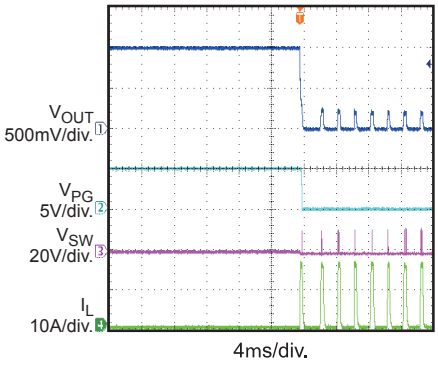
I_{OUT}=10A



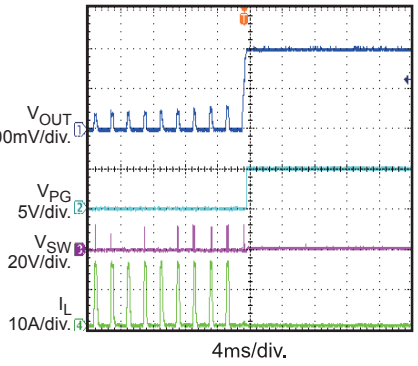
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
VIN = 12V, VOUT = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

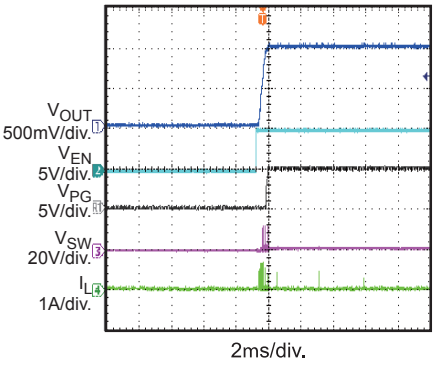
Short Entry
I_{OUT} = 0A



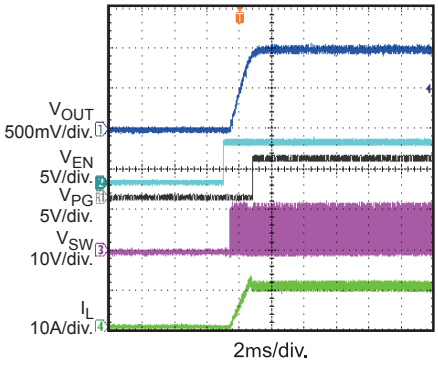
Short Recovery
I_{OUT} = 0A



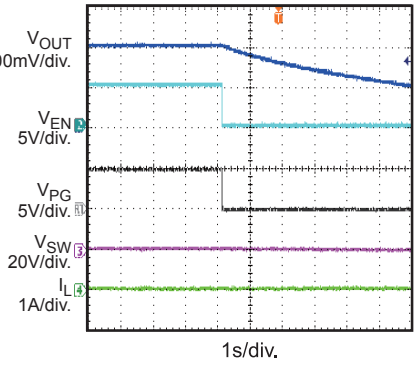
Start-Up through Enable
I_{OUT} = 0A



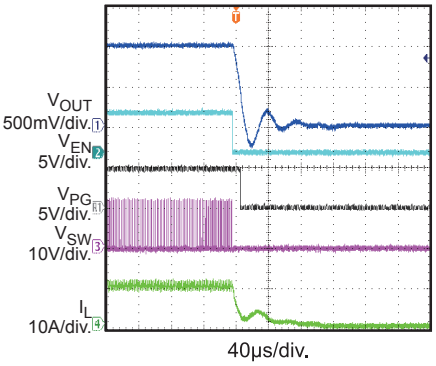
Start-Up through Enable
I_{OUT} = 10A



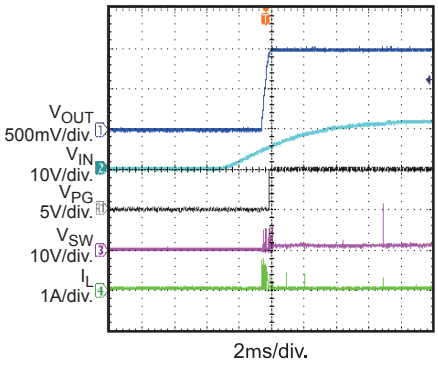
Shutdown through Enable
I_{OUT} = 0A



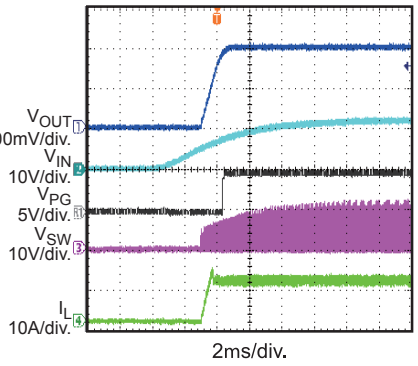
Shutdown through Enable
I_{OUT} = 10A



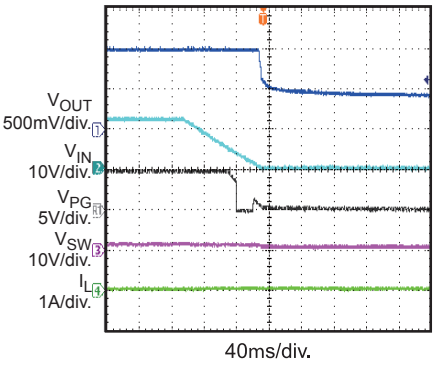
Start-Up through Input Voltage
I_{OUT} = 0A



Start-Up through Input Voltage
I_{OUT} = 10A



Shutdown through Input Voltage
I_{OUT} = 0A

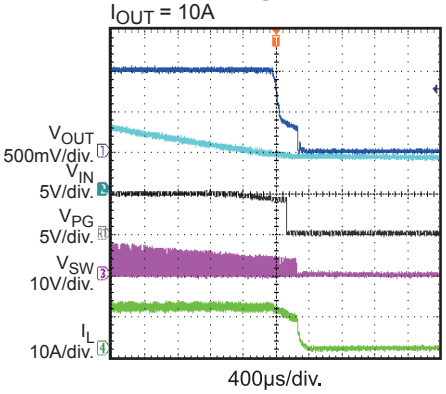


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.

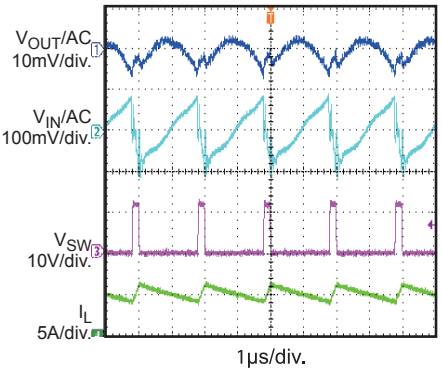
Shutdown through Input Voltage

I_{OUT} = 10A



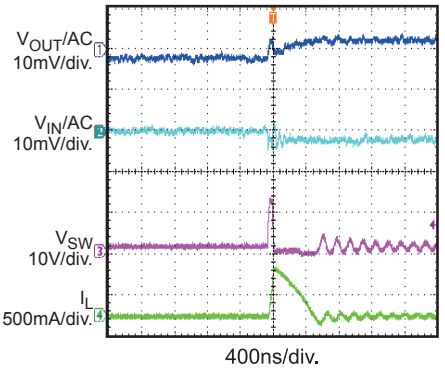
Input/Output Ripple

I_{OUT} = 10A



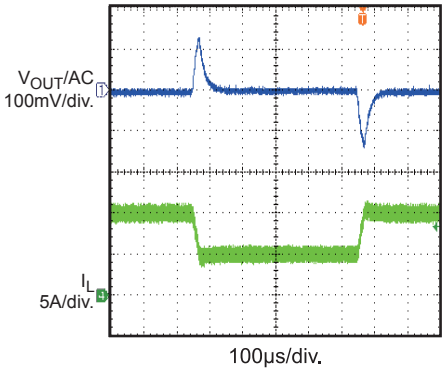
Input/Output Ripple

I_{OUT} = 0A, PFM



Load Transient Response

I_{OUT} = 5A to 10A



PIN FUNCTIONS

QFN-14 PIN#	Name	Description
1	BST	**Bootstrap.** A capacitor is required between SW and BST to form a floating supply across the high-side switch driver.
2	SW	**Switch output.** Connect SW using a wide PCB trace.
3, 4, 6	NC	**No connection.** Leave NC floating.
5	EN/SYNC	**Enable/synchronize.** Drive EN/SYNC high to enable the MP8714. EN/SYNC has an internal 6.2μA pull-up current to 5V, so the MP8714 can start-up automatically when EN/SYNC is floating. Apply an external clock to EN/SYNC to change the switching frequency.
7	PG	**Power good indication.** PG is an open-drain structure. PG switches low if the output voltage is out of regulation window. PG only indicates an under-voltage (UV) condition.
8	PGND	**System power ground.** PGND is the reference ground of the regulated output voltage. Requires special consideration during PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MP8714 operates from a 4.5V to 17V input rail. A ceramic capacitor is required to decouple the input rail. Connect VIN using a wide PCB trace.
10	VOUT	**Sense input of the output voltage.** Connect VOUT to the positive terminal of the load.
11	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage in a FB control loop.
12	SS	**Soft start.** Connect a capacitor from SS to ground to set the soft-start time.
13	VCC	**Internal LDO regulator output.** Decouple VCC with a 0.47μF capacitor.
14	AGND	**Signal ground.** AGND is not internally connected to system ground directly. Ensure that AGND is connected to system ground during PCB layout.

BLOCK DIAGRAM

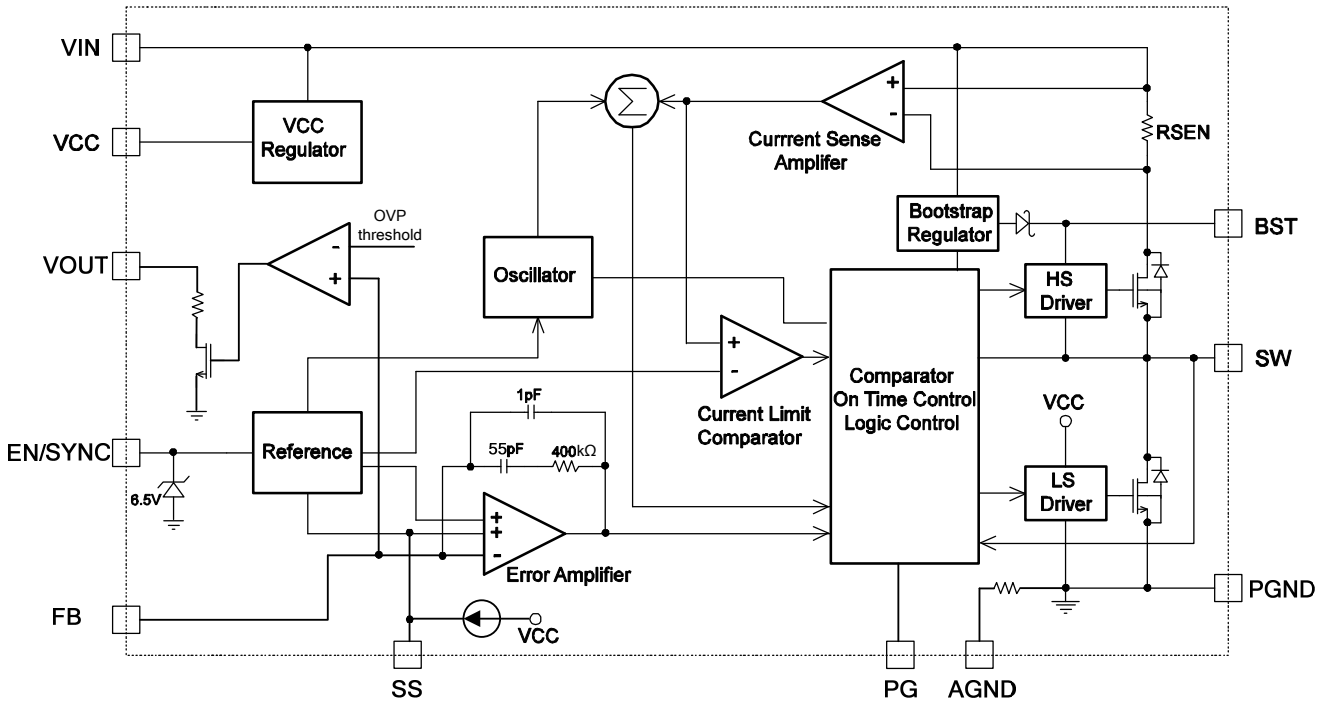


Figure 1: Functional Block Diagram

OPERATION

The MP8714 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MP8714 offers a very compact solution that achieves 10A of output current with excellent load and line regulation over a wide input supply range.

The MP8714 has three working modes: continuous conduction mode (CCM), advanced asynchronous modulation (AAM) mode, and discontinuous conduction mode (DCM).

CCM Control Operation

In continuous conduction mode (CCM), the internal clock initiates a pulse-width modulation (PWM) cycle. The high-side MOSFET (HS-FET) turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage (V_{COMP}). After a period of dead time, the low-side MOSFET (LS-FET) turns on and remain on until the next clock cycle begins. The MP8714 repeats this operation in every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} (500kHz switching frequency) within 95% of one PWM period, the HS-FET is forced off.

AAM Control Operation

In light-load condition, the MP8714 works in advanced asynchronous modulation (AAM) mode (see Figure 2). V_{AAM} is an internal, fixed voltage when the input and output voltages are fixed. V_{COMP} is the error amplifier output which represents peak inductor current information. When V_{COMP} is lower than V_{AAM}, the internal clock is blocked, so the MP8714 skips some pulses and achieves light-load power save. Refer to the related application note (AN032) for more detail.

The internal clock resets whenever V_{COMP} is higher than V_{AAM}. Simultaneously, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light-load feature in this device is optimized for 12V input applications.

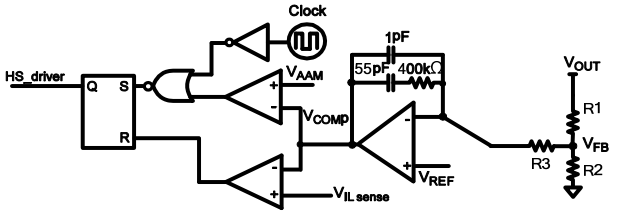


Figure 2: Simplified AAM Control Logic

DCM Control Operation

V_{COMP} ramps up with the increasing output current. When its minimum value exceeds V_{AAM}, the MP8714 enters discontinuous conduction mode (DCM) (see Figure 3). In this mode, the internal clock initiates the PWM cycle. The HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. After a period of dead time, the LS-FET turns on and remain on until the inductor current value decreases to zero. The MP8714 repeats this same operation in every clock cycle to regulate the output voltage.

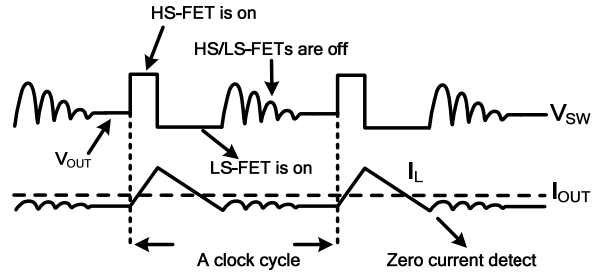


Figure 3: DCM Control Operation

VCC Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output voltage decreases and follows the input voltage. A 0.47μF ceramic capacitor is required for decoupling purposes.

Error Amplifier (EA)

The error amplifier compares the FB voltage with the internal 0.6V reference (REF) and outputs a COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation

networkminimizes the external component count and implifies control loop design.

Enable Control (EN/SYNC)

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator; drive EN/SYNC low to turn off the regulator. An internal 6.2μA pull-up current to a 5V power supply allows for automatic start-up when EN/SYNC is floating.

EN/SYNC is clamped internally using a 5.7V series Zener diode (see Figure 4). Connecting the EN/SYNC input through a pull-up resistor to the voltage on VIN limits the EN/SYNC input current to less than 100μA.

For example, with 12V connected to VIN, $R_{PULLUP} \geq (12V - 5.7V) \div 100\mu A = 63k\Omega$.

Connecting EN/SYNC to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤5.5V to prevent damage to the Zener diode.

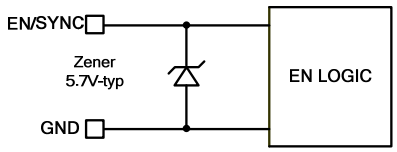


Figure 4: 5.7V Zener Diode Connection

For external clock synchronization, connect a clock with a frequency range between 200kHz and 2MHz to EN/SYNC. The internal clock rising edge synchronizes with the external clock rising edge once the external clock is present. Set the external clock signal with a pulse width less than 80% of one internal clock cycle time.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8714 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4.16V, while its falling threshold is 3.55V.

Soft Start (SS)

The MP8714 employs a soft start (SS) mechanism to ensure smooth output during power-up. When EN/SYNC becomes high, an internal current source (10μA) charges up the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it continues ramping up while V_{REF} takes over the PWM comparator. At this point, the soft start finishes and MP8714 enters into steady-state operation.

The SS capacitor value can be determined with Equation (1):

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

If the output capacitors have a large capacitance value, do not set the SS time to be too small; otherwise, the current limit can be easily reached during SS.

Pre-Bias Start-Up

The MP8714 has been designed for monotonic start-up into a pre-biased output voltage. If the output is pre-biased to a certain voltage during start-up, the voltage on the soft-start capacitor is charged. When the soft-start capacitor's voltage exceeds the sensed output voltage at FB, the part turns on the high-side and low-side power switches sequentially. The output voltage begins to ramp up following the soft-start slew rate.

Power Good (PG) Indicator

The MP8714 uses a power good (PG) output to indicate whether the output voltage of the module is ready or not. PG is an open-drain output. Connect PG to VCC or another voltage source through a pull-up resistor (e.g.: 100kΩ). When the input voltage is applied, PG is pulled down to GND. When V_{FB} is above 90% of V_{REF}, PG is pulled high after a 100μs delay. During normal operation, PG is pulled low when V_{FB} drops below 70% of V_{REF} after a 100μs delay.

When UVLO or OTP occurs, PG is pulled low immediately. When over-current (OC) occurs, PG is pulled low when V_{FB} drops below 70% of V_{REF} after a 100μs delay.

PG does not respond to an output over-voltage condition.

Output Over-Voltage Protection (OVP)

detect an over-voltage event. When the feedback voltage rises higher than 120% of the internal reference voltage, the controller enters linear discharge mode. During this period, a 35Ω resistor connected between VOUT and ground discharges the output and keeps it within the normal range. Once the output voltage falls below 105% of the reference, the controller exits linear discharge mode.

Over-Current Protection (OCP) and Hiccup

The MP8714 has a cycle-by-cycle over-current limit. When the inductor current peak value exceeds the set current limit threshold, the HS-FET turns off, and the LS-FET turns on and remains on until the inductor current falls below the internal valley current limit threshold. The valley current limit circuit is employed to decrease the operation frequency after the peak current limit threshold is triggered.

Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (typically 30% below the reference). Once UV is triggered, the MP8714 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP8714 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature is below its lower threshold (typically 140°C), the chip is enabled again.

The MP8714 monitors both FB and VOUT to

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN through D1, M1, C5, L1, and C2 (see Figure 5). If VIN - V_{SW} exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C5.

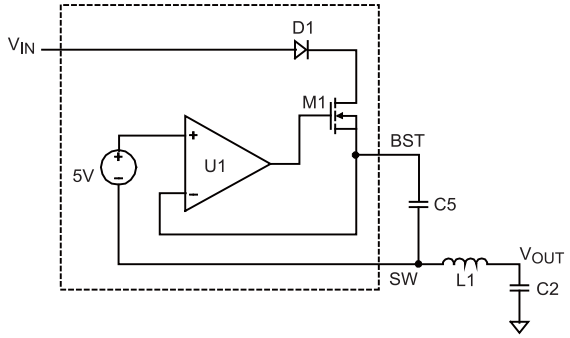


Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both VIN and EN/SYNC exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN/SYNC low, VIN low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output

The reference voltage and external resistor divider can set the output voltage through FB. The feedback resistors R1 and R3 set the feedback loop bandwidth with the internal compensation capacitor. Choose a value for R1 first, and then calculate R2 with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{REF}} - 1} \quad (2)$$

The T-type network is highly recommended (see Figure 6).

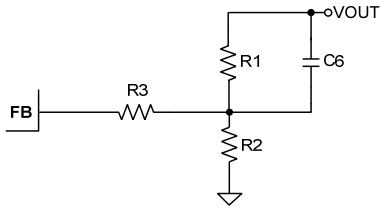


Figure 6: T-Type Network

Table 1 lists the recommended feedback resistors value for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (9)

VOUT (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	C6 (pF)	L (μH)
0.9	80.6 (1%)	162 (1%)	51 (1%)	22	1.5
1.0	80.6 (1%)	120 (1%)	51 (1%)	22	1.5
1.2	80.6 (1%)	80.6 (1%)	40.2 (1%)	22	1.5
2.5	60.4 (1%)	19.1 (1%)	30 (1%)	22	2.2
3.3	60.4 (1%)	13.3 (1%)	20 (1%)	33	3.3
5	60.4 (1%)	8.25 (1%)	20 (1%)	33	3.3

NOTE:

9) The recommended parameters are based on a 12V input voltage and 22μFx4 output capacitor. Different input voltage and output capacitor values may affect the selection of R1, R2, R3, and C6. For other components' parameters, please refer to the Typical Application Circuits on page 18.

Selecting the Inductor

Use a 0.47μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current for most applications. For the highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended for best results because of their low ESR and small temperature coefficients. For most applications, use two 22μF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at VIN = 2VOUT, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (8)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated by Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8714 can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guidelines [10]

Efficient PCB layout is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 7 and follow the guidelines below.

1. Place the high current paths (PGND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Keep the VIN and GND pads connected with large copper traces.
3. Use at least two layers for the VIN and GND trace to achieve better thermal performance.
4. Add several vias close to the VIN and GND pads to help with thermal dissipation.
5. Place the input capacitors as close to VIN and GND as possible.
6. Place the decoupling capacitor as close to VCC and GND as possible.
7. Place the external feedback resistors next to FB.
8. Ensure that there is no via on the FB trace.
9. Keep the switching node SW short and away from the feedback network.
10. Keep the BST voltage path (BST, C5, and SW) as short as possible.

NOTE:

10) The recommended layout is based on the Typical Application circuit on page 18.

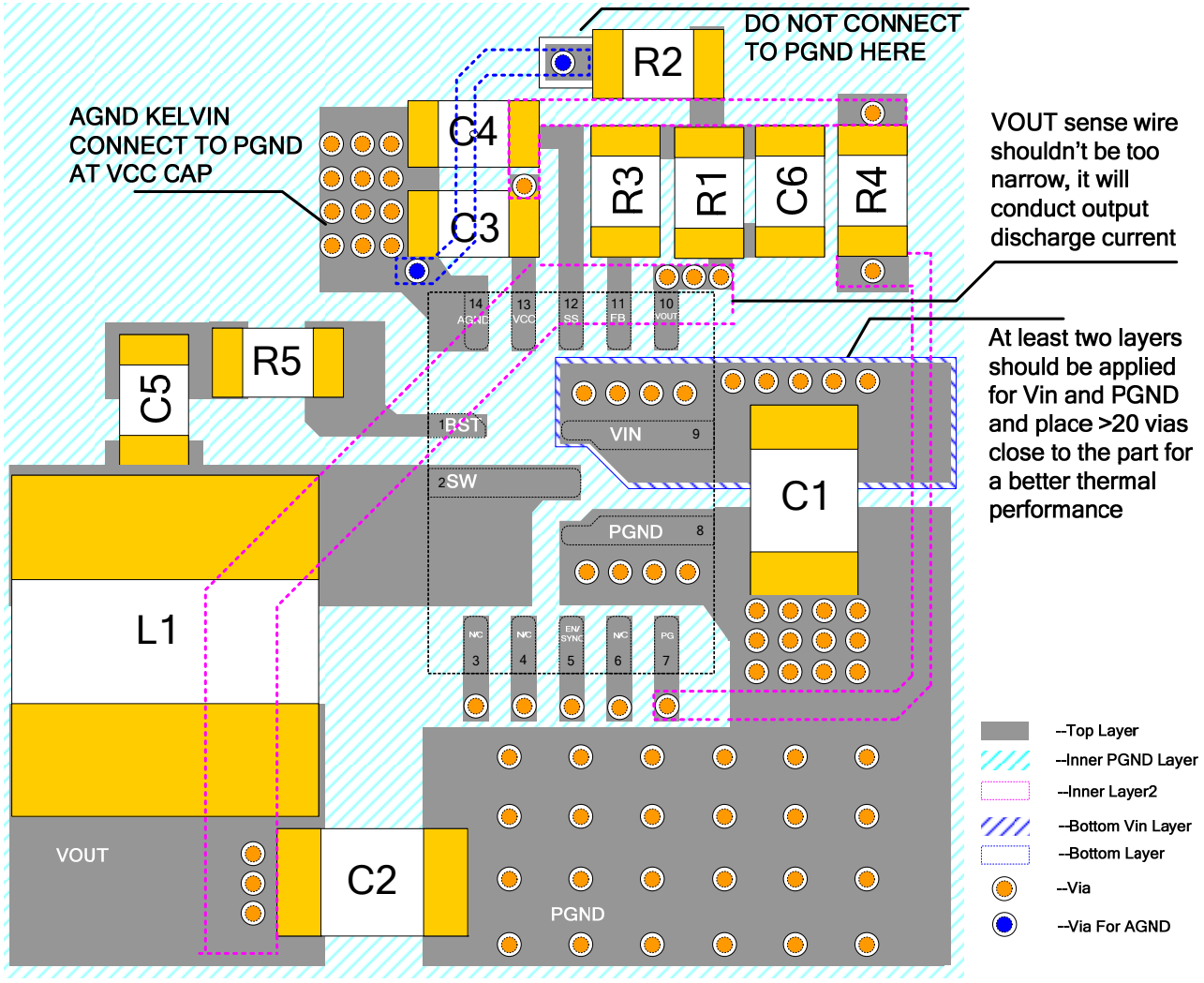


Figure 7: Recommended Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below.

Table 2: Design Example

VIN	12V
VOUT	1V
I_{OUT}	10A

The detailed application schematics are shown in Figure 8 through Figure 13. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

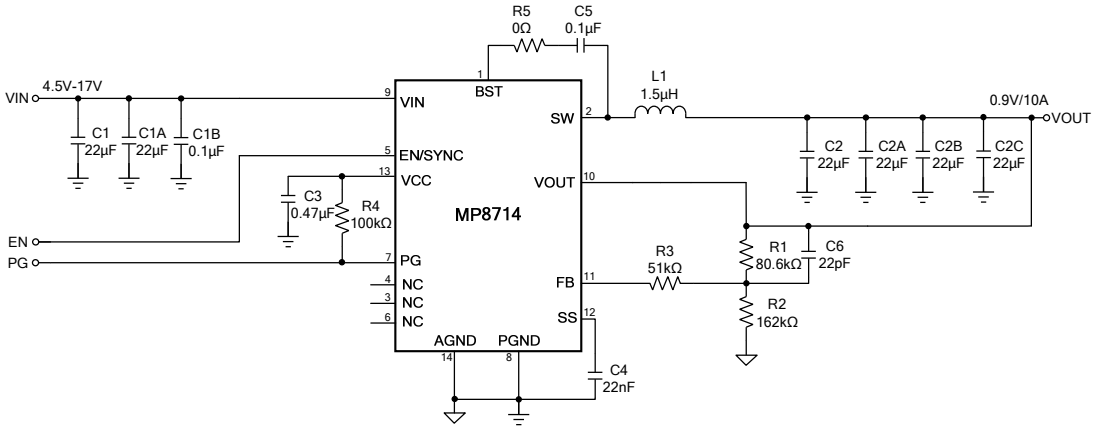


Figure 8: VIN = 4.5 - 17V, VOUT = 0.9V, I_{OUT} = 10A

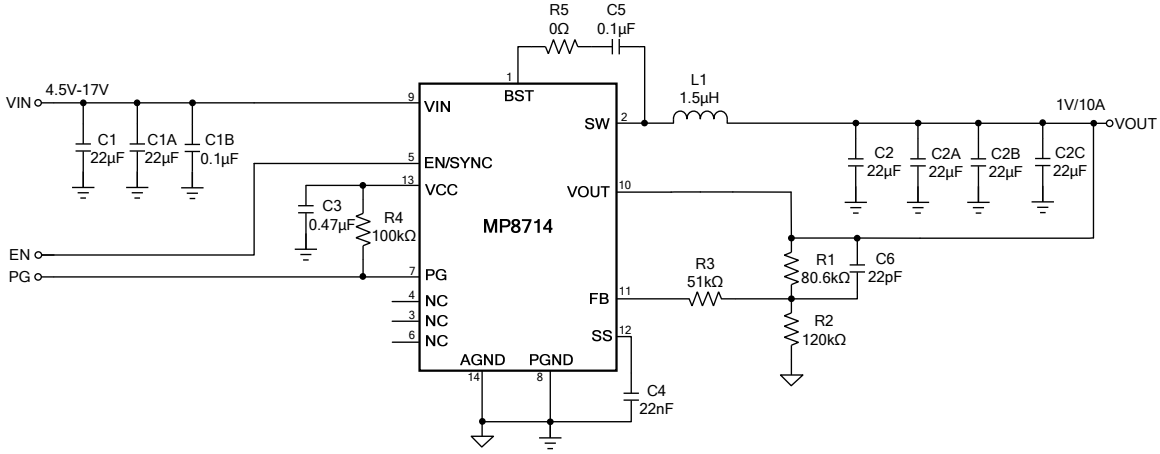


Figure 9: VIN = 4.5 - 17V, VOUT = 1V, I_{OUT} = 10A

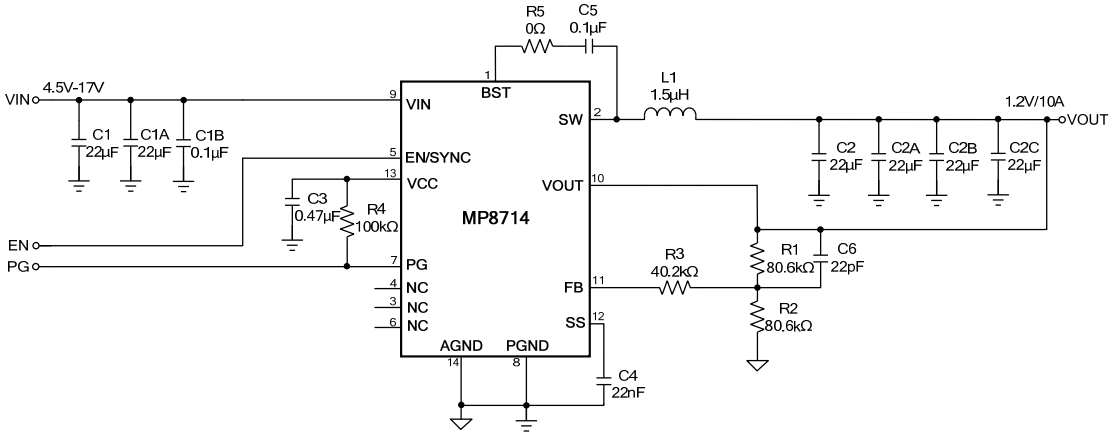


Figure 10: VIN = 4.5 - 17V, VOUT = 1.2V, I_{OUT} = 10A

Typical Application Circuits *(CONTINUED)*

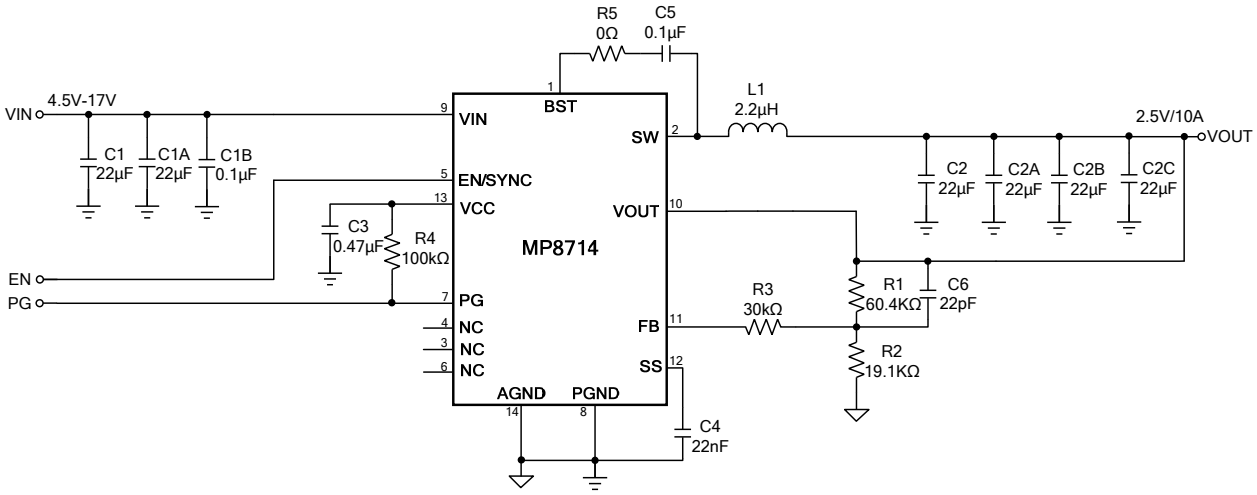


Figure 11: VIN = 4.5 - 17V, VOUT = 2.5V, I_{OUT} = 10A

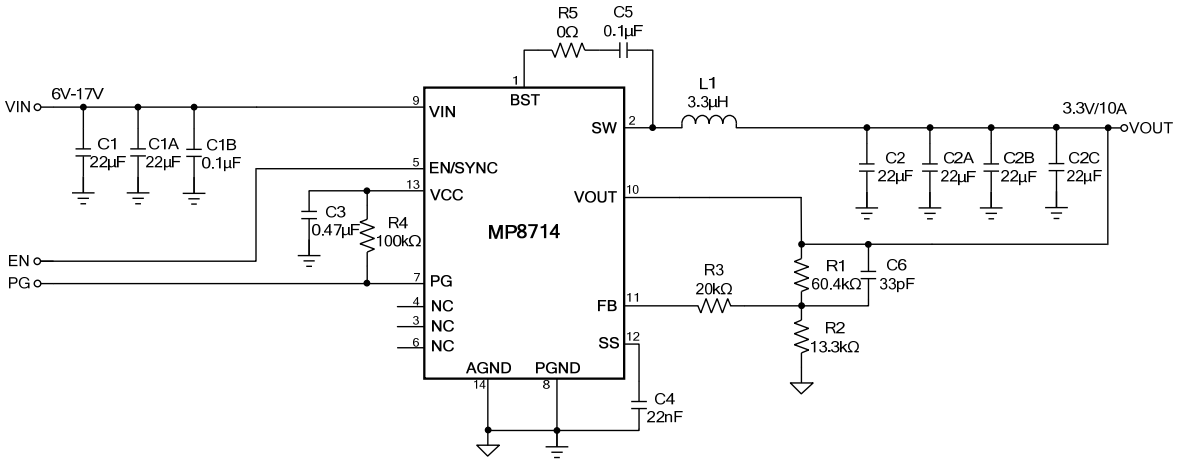


Figure 12: VIN = 6 - 17V, VOUT = 3.3V, I_{OUT} = 10A (11)

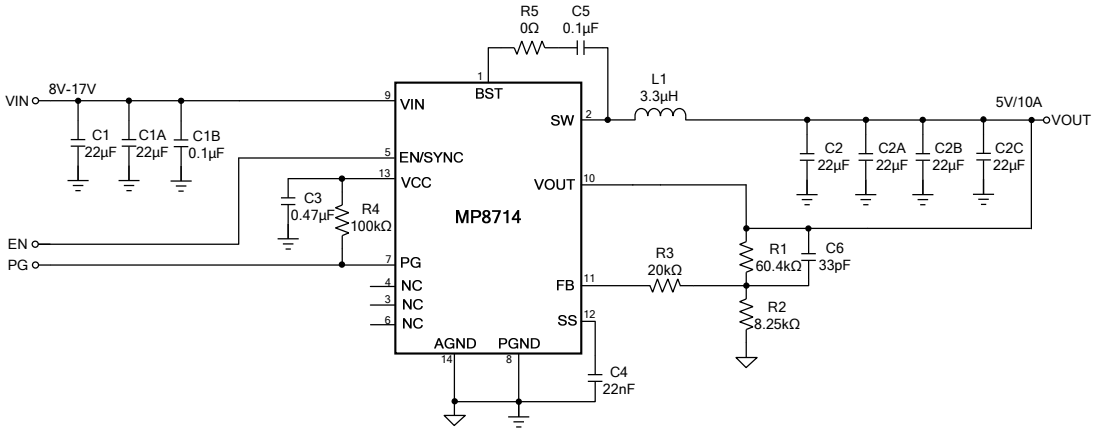


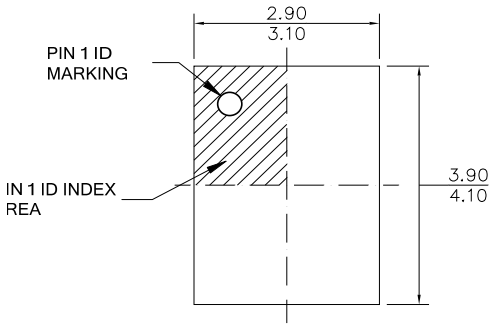
Figure 13: VIN = 8 - 17V, VOUT = 5V, I_{OUT} = 10A (11)

NOTE:

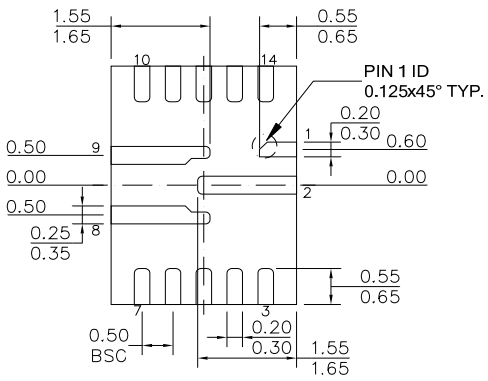
11) Based on the evaluation board test results at 25ºC ambient temperature, a lower input voltage will trigger over-temperature protection at full load.

PACKAGE INFORMATION

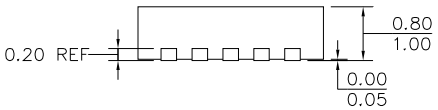
QFN-14 (3mmx4mm)



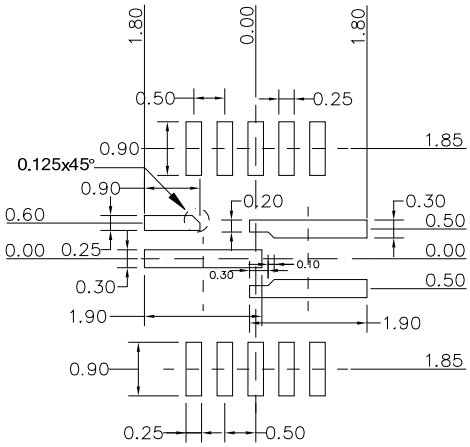
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMET MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.