For most applications, a 22µF ceramic capacitor is sufficient to maintain the DC input voltage. It is strongly recommended to use another lower value capacitor (e.g.: 1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to IN and GND as possible (see PCB Layout Guidelines on page 18).

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

With tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4423A can be optimized for a wide range of capacitance and ESR values.

BST Resistor and External BST Diode

A 20Ω resistor in series with a BST capacitor is recommended to reduce SW voltage spikes. A higher resistance is better for SW spike reduction but compromises efficiency.

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high (>65%). A power supply between 2.5V and 5V can be used to power the external bootstrap diode. Either VCC or VOUT can be used as the power supply in this circuit (see Figure 6).

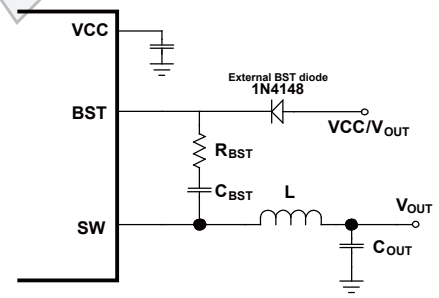


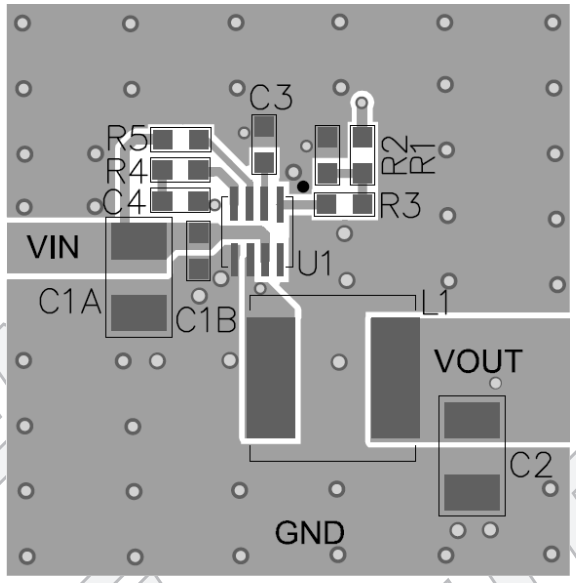
Figure 6: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1µF to 1µF.

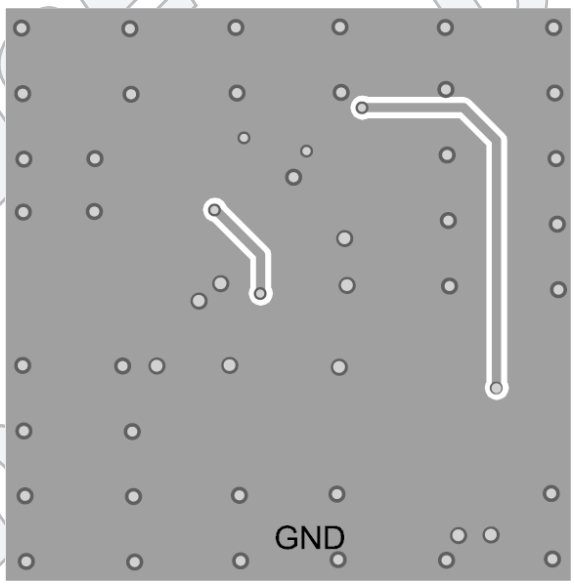
PCB Layout Guidelines

Efficient PCB layout, especially the input capacitor and VCC capacitor placement, is critical for stable operation. For best results, refer to Figure 7 and follow the guidelines below.

1. Place the ceramics input capacitor as close to IN and GND as possible, especially the small package size (0603) input bypass capacitor.
2. Keep the connection of the input capacitor and IN as short and wide as possible.
3. Place the VCC capacitor to VCC and GND as close as possible.
4. Make the trace length of VCC to the capacitor to GND as short as possible.
5. Use a large ground plane connected directly to GND.
6. Add vias near GND if the bottom layer is the ground plane.
7. Route SW and BST away from sensitive analog areas such as FB.
8. Place the T-type feedback resistor close to the chip to ensure that the trace connecting to FB is as short as possible.



Top Layer



Bottom Layer

Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

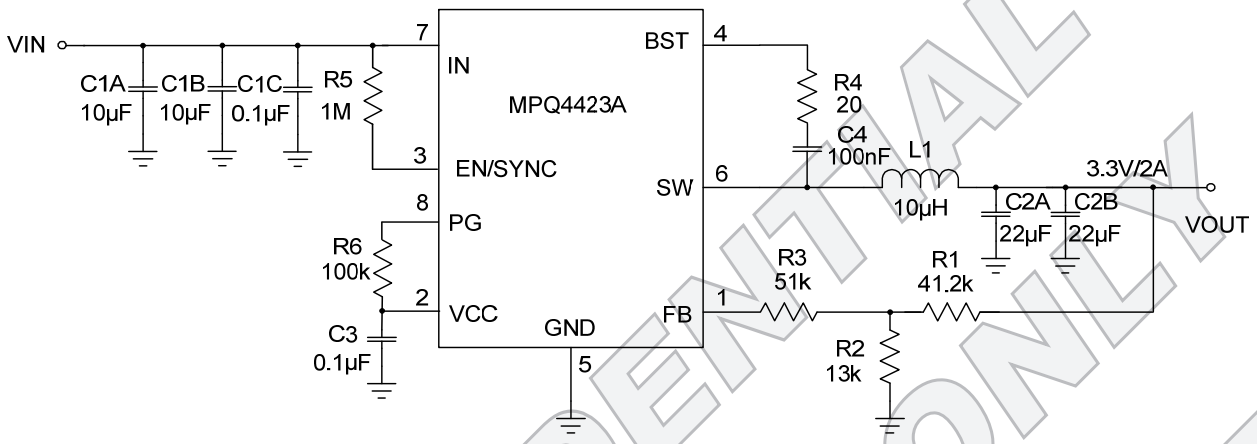
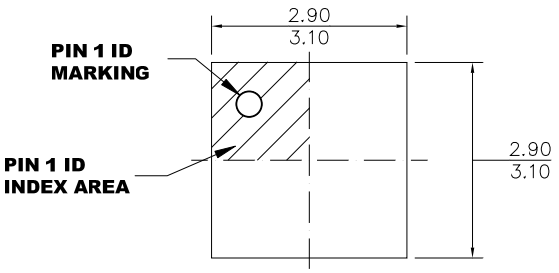


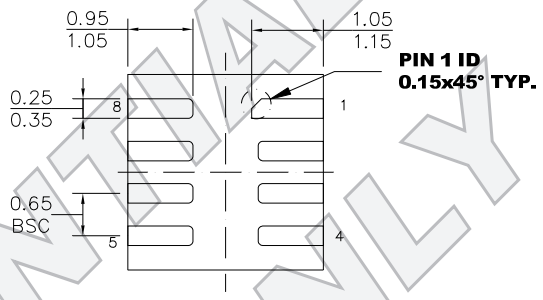
Figure 8: 3.3V Output Typical Application Circuit

PACKAGE INFORMATION

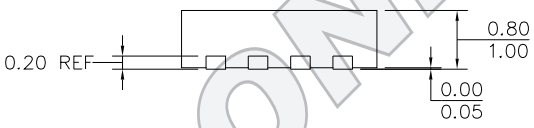
QFN-8 (3mmx3mm)



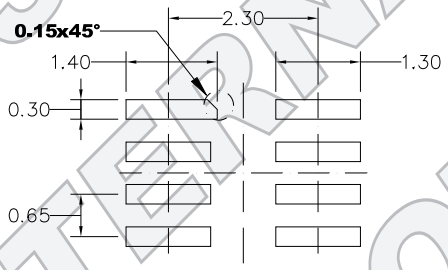
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.