The Future of Analog IC Technology®

MPQ8616

High Efficiency, 6A/12A, 6V Synchronous Step-down Converter

DESCRIPTION

The MPQ8616 is fully integrated high frequency synchronous rectified step-down switch mode converter. It offers very compact solutions to achieve 6A/12A output current from a 3V to 6V input with excellent load and line regulation.

Constant-On-Time (COT) control mode provides fast transient response and eases loop stabilization. The MPQ8616 can operate with a low-cost electrolytic capacitor and can support ceramic output capacitor with external slope compensation.

Operating frequency is programmed by an external resistor and is compensated for variations in V_{IN}. It is almost constant with all the input voltage and output load conditions.

Under voltage lockout is internally set at 2.8 V, but can be increased by programming the threshold with a resistor network on the enable pin. The output voltage startup ramp is controlled by the soft start pin. A power good signal indicates the output is within its nominal voltage range.

Full fault protection including OCP, SCP, OVP UVP and OTP is provided by internal comparators.

The MPQ8616 requires a minimum number of readily available standard external components and are available in QFN3x4 packages.

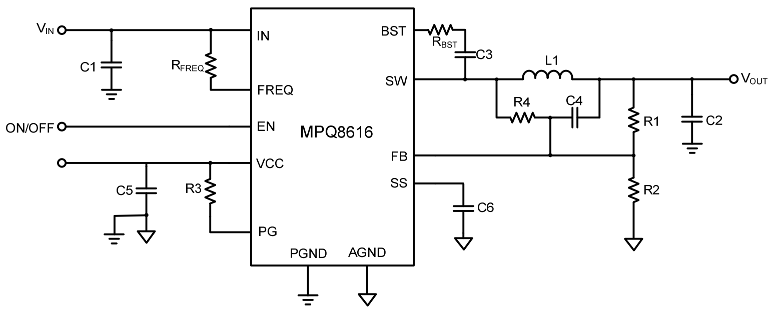
FEATURES

- 1.5V to 6V Wide Input Range
- 3 V to 6V VCC Operating Supply
- 6A/12A Output Current
- Low R_{DS}(ON) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive COT for Ultrafast Transient Response
- 1% Reference Voltage Over -20°C to +85°C Junction Temperature Range
- Programmable Soft Start Time
- Pre-Bias Start up
- Programmable Switching Frequency from 300kHz to 1MHz.
- Minimum On Time T_{ON_MIN}=60ns
  Minimum Off Time T_{OFF_MIN}=100ns
- Non-latch OCP, non-latch OVP Protection and Thermal Shutdown
- Output Adjustable from 0.61V to 4.5V

APPLICATIONS

- Telecom System Base Stations
- Networking Systems
- Server
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION



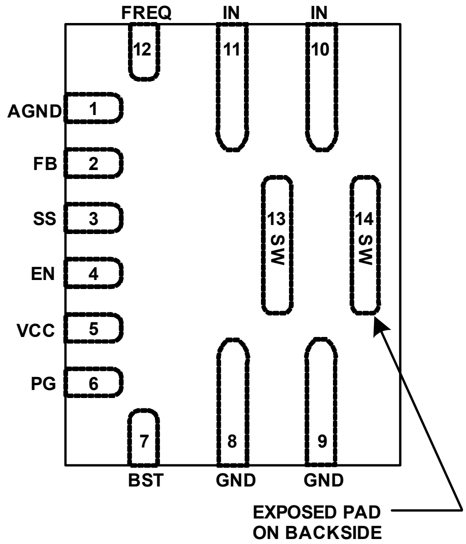
ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ8616GL-6	QFN (3x4mm)	MP8616 6
MPQ8616GL-12	QFN (3x4mm)	MP8616 12

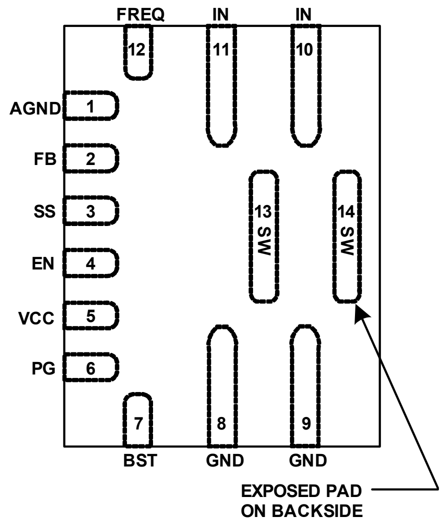
* For Tape & Reel, add suffix –Z (e.g. MPQ8616GL-6/12–Z);

PACKAGE REFERENCE

TOP VIEW



TOP VIEW



Part Number**	Package	Part Number**	Package
MPQ8616GL-6	QFN14 (3x4mm)	MPQ8616GL-12	QFN14 (3x4mm)
** For Tape & Reel, add suffix –Z (eg. MPQ8616GL-6–Z)		*** For Tape & Reel, add suffix –Z (eg. MPQ8616GL-12–Z)	

ABSOLUTE MAXIMUM RATINGS [(1)]

Supply Voltage V_{IN} 6.5V
V_{SW} .... -0.3V to V_{IN} + 0.3V
V_{SW} (30ns)................................... -3V to V_{IN} + 3V
V_{IN} -V_{SW} .... -0.3V to V_{IN} + 0.3V
V_{IN} -V_{SW} (30ns) .... -3V to V_{IN} + 3V
V_{BST}..V_{SW} + 6V
All Other Pins .... -0.3V to +6V
Continuous Power Dissipation (T_A=+25°) [(2)]……
QFN(3x4mm)…………………...……………2.6W
Junction Temperature .... 150°C
Lead Temperature .... 260°C
Storage Temperature................-65°C to +150°C

Recommended Operating Conditions [(3)]

Input Supply Voltage V_{IN} .... 1.5V to 6V
VCC Supply Voltage V_{cc} .... 3V to 6V
Output Voltage V_{OUT}...................... 0.61V to 4.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance [(4)]

	θ_{JA}	θ_{JC}	
QFN (3mmx4mm)	48	10	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40 to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		1	2	μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V	0.6	1.05	1.3	mA
MOSFET						
High-side Switch On Resistance	HS_{RDS-ON}	MPQ8616-6, T_J =25°C		19.8		mΩ
		MPQ8616-12, T_J =25°C		16		
Low-side Switch On Resistance	LS_{RDS-ON}	MPQ8616-6 T_J =25°C		15.3		mΩ
		MPQ8616-12, T_J =25°C		8.4		
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 5V		0.01	3	μA
Current Limit						
High-side Current Limit	I_{LIMIT}	MPQ8616-6	9.5	12	14.5	A
		MPQ8616-12	17	23	27	
Timer						
One-Shot On Time	t_{ON}	R_{FREQ}=165kΩ,V_{OUT}=1.2V		200		ns
Minimum Off Time	t_{OFF}		50	100	150	ns
Fold back Timer(5)	$t_{FOLDBACK}$	OCP happens		2.5		μs
Over-voltage and Under-voltage Protection						
OVP Threshold	V_{OVP}		110%	120%	130%	V
OVP Delay(5)	t_{OVP}			1		μs
UVP Threshold(5)	V_{UVP}			50%		V_{REF}
Reference And Soft Start						
Reference Voltage	V_{REF}	T_J = -20°C to +85°C	604	610	616	mV
		T_J = -40°C to +125°C	601	610	619	
Feedback Current	I_{FB}	V_{FB} = 610mV		0.001	150	nA
Soft Start Charging Current	I_{SS}	V_{SS}=0V	5	7.5	10	μA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40 to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable And UVLO						
Enable Input Low Voltage	VIL_{EN}		1.4		1.8	V
Enable Hysteresis	V_{EN-HYS}			890		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		1.5	2	μA
		V_{EN} = 0V		0.01	1	
VCC UVLO						
VCC Under Voltage Lockout Threshold Rising	VCC_{Vth}		2.3	2.8	2.95	V
VCC Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}			300		mV
Power Good						
Power Good Rising Threshold	PG_{Vth-Hi}		84%	90%	96%	V_{REF}
Power Good Falling Threshold	PG_{Vth-Lo}		63%	70%	73%	V_{REF}
Power Good Deglitch Timer	PG_{Td}	T_{SS}=1ms,		2000	5000	μs
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V		50	150	nA
Thermal Protection						
Thermal Shutdown	T_{SD}	Note 5	150	160		°C
Thermal Shutdown Hysteresis				25		°C

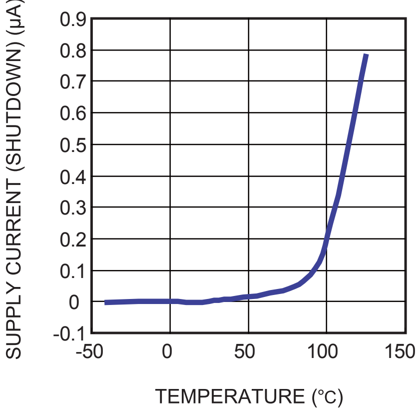
Note:

5) Guaranteed by design.

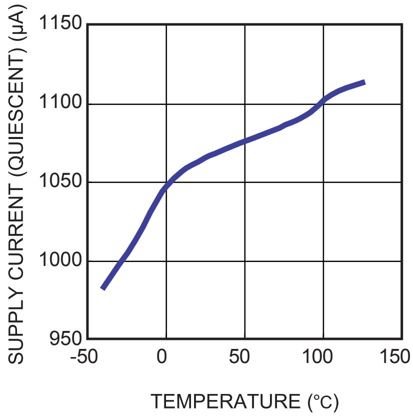
TYPICAL CHARACTERISTICS

MPQ8616, Performance waveforms are tested on the evaluation board of the Design Example section.

Supply Current (Shutdown) vs. Temperature

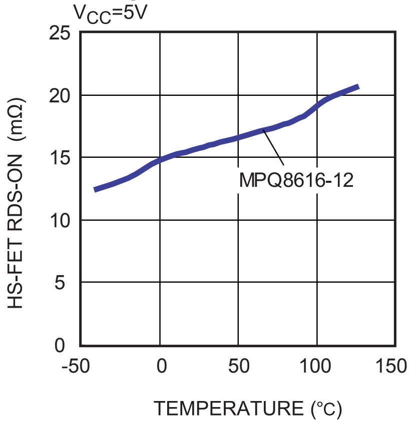


Supply Current (Quiescent) vs. Temperature



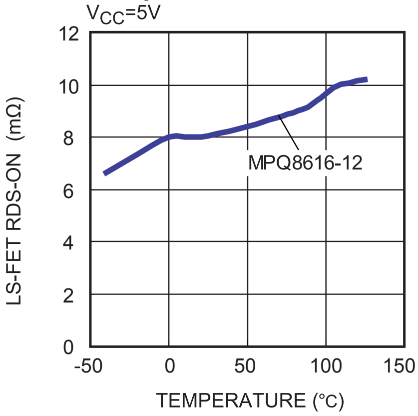
HS-FET R_{DS-ON} vs. Temperature

V_{CC}=5V

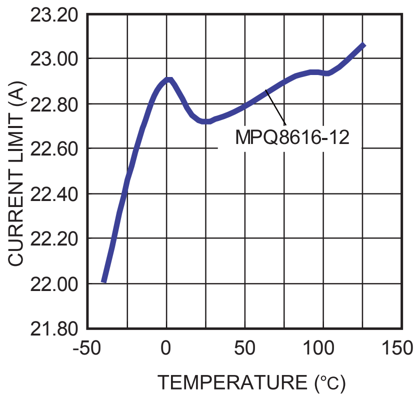


LS-FET R_{DS-ON} vs. Temperature

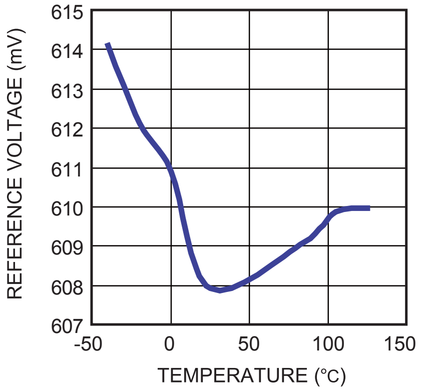
V_{CC}=5V



HS-FET Current Limit vs. Temperature

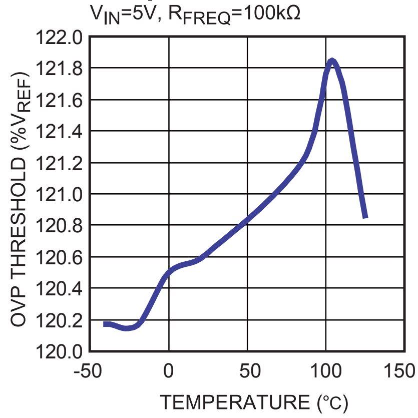


Reference Voltage vs. Temperature



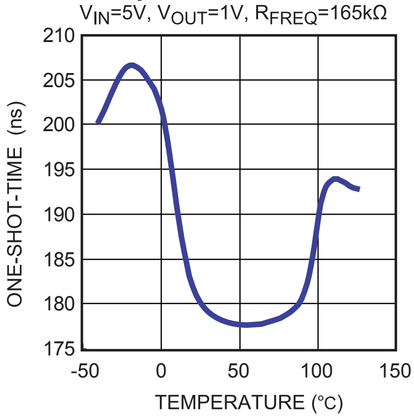
OVP Threshold vs. Temperature

V_{IN}=5V, R_{FREQ}=100kΩ



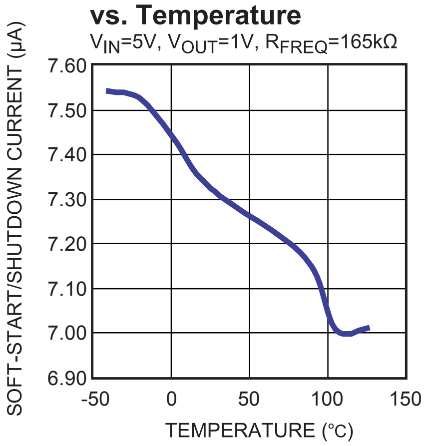
One-Shot-Time vs. Temperature

V_{IN}=5V, V_{OUT}=1V, R_{FREQ}=165kΩ



Soft-Start/Shutdown Current vs. Temperature

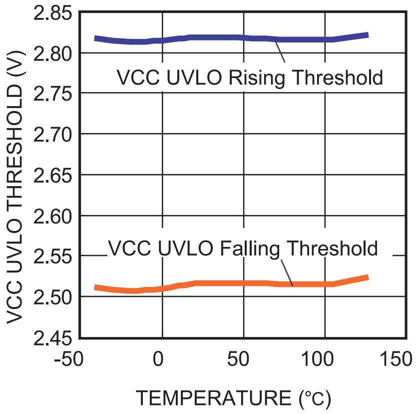
V_{IN}=5V, V_{OUT}=1V, R_{FREQ}=165kΩ



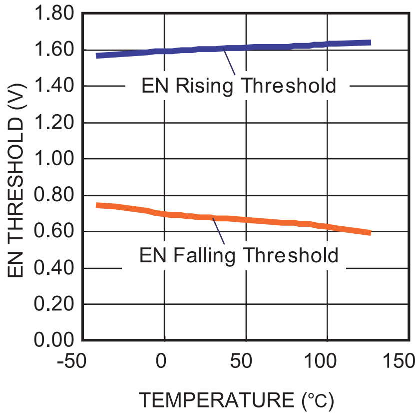
TYPICAL CHARACTERISTICS *(continued)*

MPQ8616GL, Performance waveforms are tested on the evaluation board of the Design Example section.

VCC UVLO Threshold vs. Temperature



EN Threshold vs. Temperature

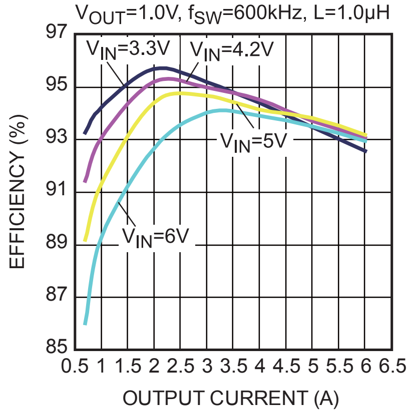


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section. MPQ8616GL-6, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

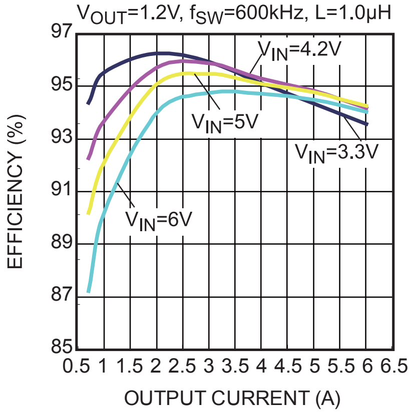
Efficiency

V_{OUT}=1.0V, f_{SW}=600kHz, L=1.0µH



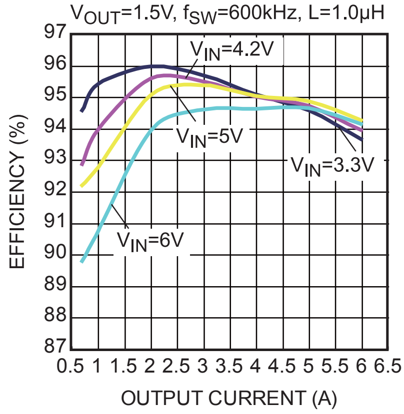
Efficiency

V_{OUT}=1.2V, f_{SW}=600kHz, L=1.0µH



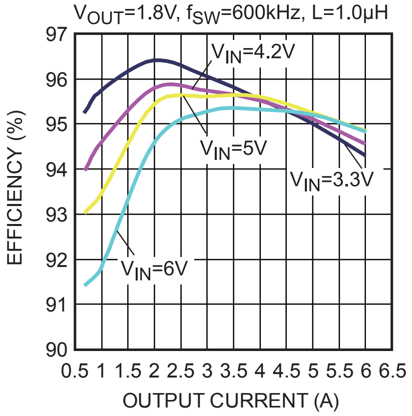
Efficiency

V_{OUT}=1.5V, f_{SW}=600kHz, L=1.0µH



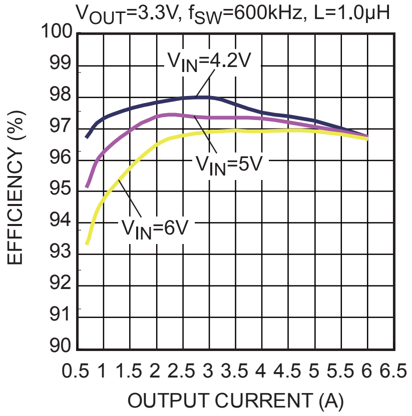
Efficiency

V_{OUT}=1.8V, f_{SW}=600kHz, L=1.0µH



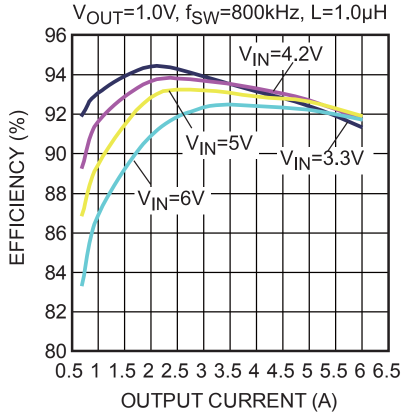
Efficiency

V_{OUT}=3.3V, f_{SW}=600kHz, L=1.0µH



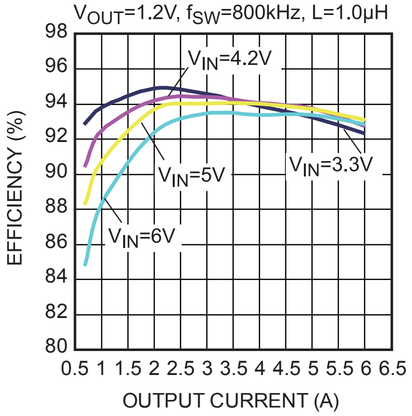
Efficiency

V_{OUT}=1.0V, f_{SW}=800kHz, L=1.0µH



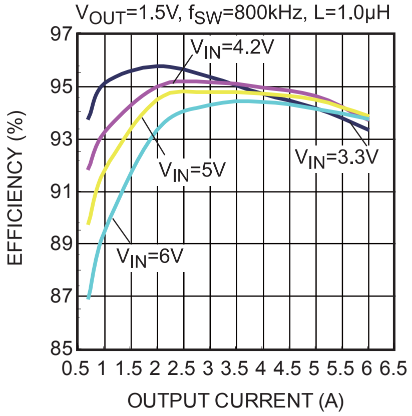
Efficiency

V_{OUT}=1.2V, f_{SW}=800kHz, L=1.0µH



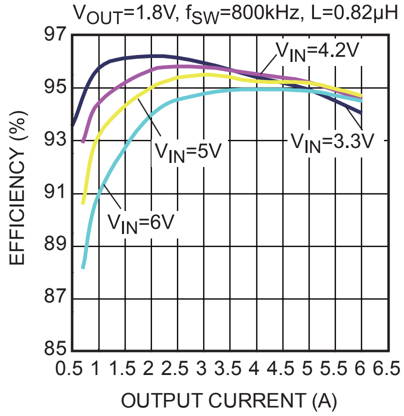
Efficiency

V_{OUT}=1.5V, f_{SW}=800kHz, L=1.0µH



Efficiency

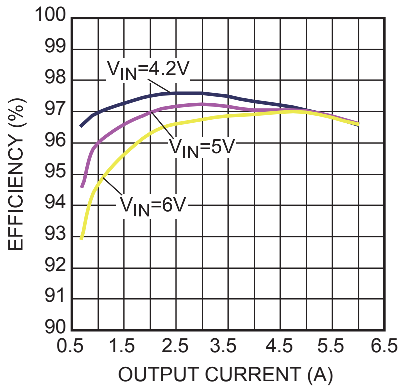
V_{OUT}=1.8V, f_{SW}=800kHz, L=0.82µH



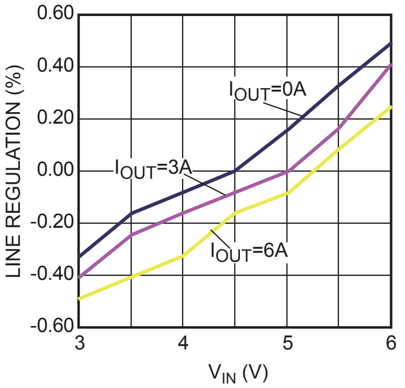
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. MPQ8616GL-6, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

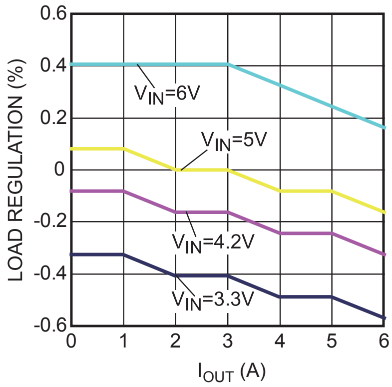
Efficiency
V_{OUT}=3.3V, f_{SW}=800kHz, L=1.0µH



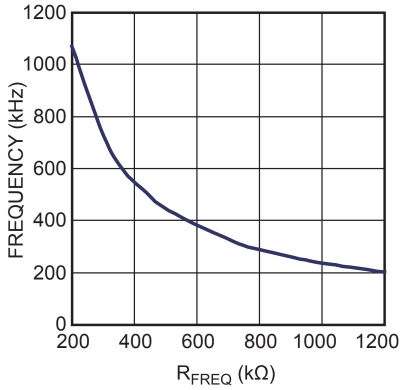
Line Regulation



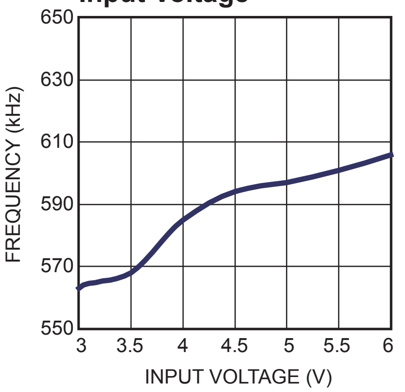
Load Regulation



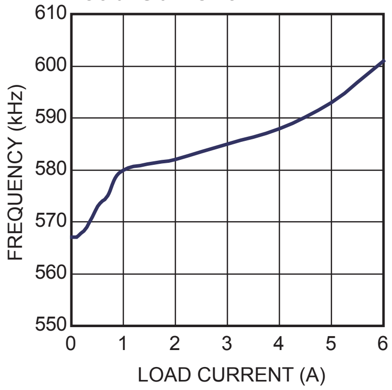
Frequency vs. R_{FREQ}



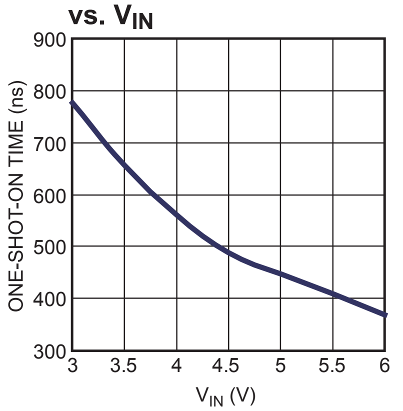
Frequency vs. Input Voltage



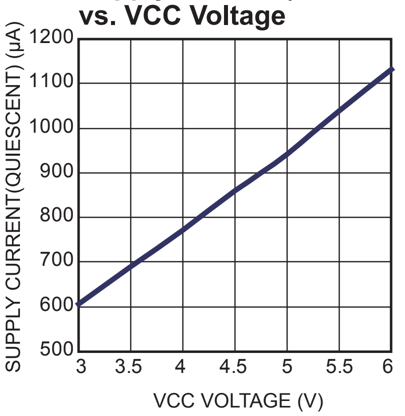
Frequency vs. Load Current



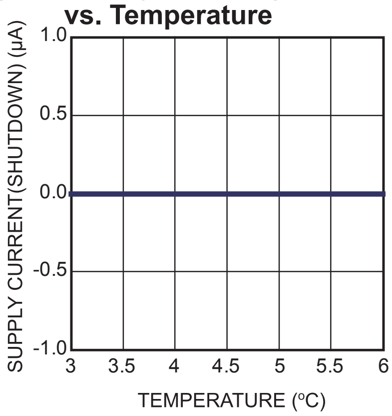
One-Shot-On Time vs. V_{IN}



Supply Current (Quiescent) vs. VCC Voltage



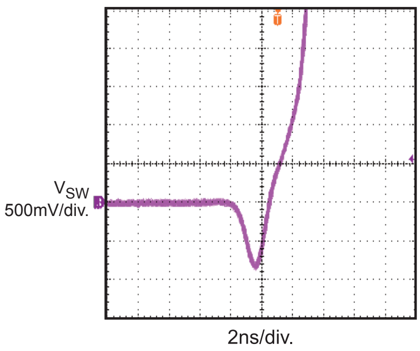
Supply Current (Shutdown) vs. Temperature



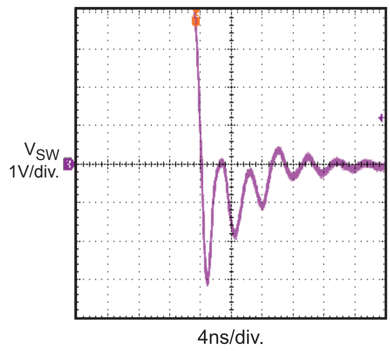
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. MPQ8616GL-6, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

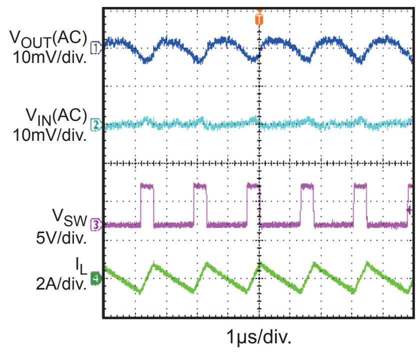
Dead Time (on)
I_{OUT} = 6A



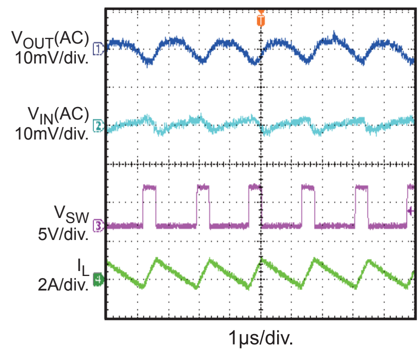
Dead Time (off)
I_{OUT} = 6A



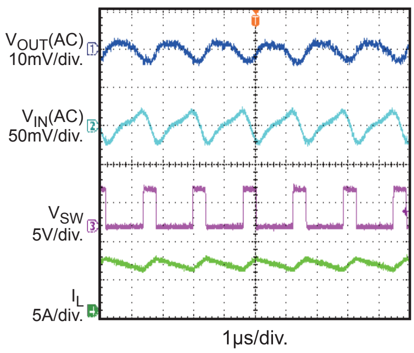
Input/Output Voltage Ripple
I_{OUT} = 0A



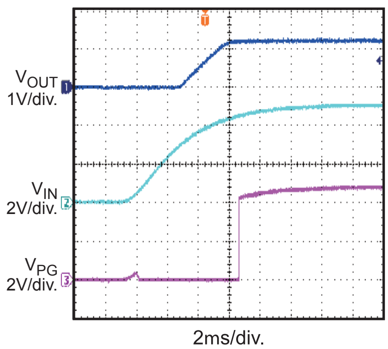
Input/Output Voltage Ripple
I_{OUT} = 0.3A



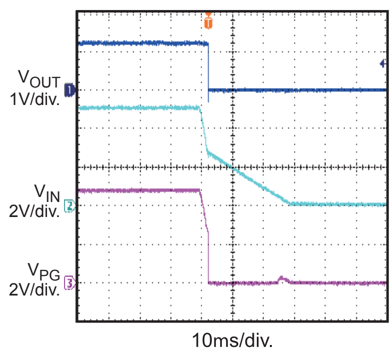
Input/Output Voltage Ripple
I_{OUT} = 6A



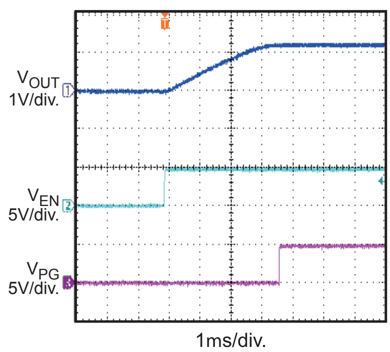
Power Good through V_{IN} Start-Up
I_{OUT} = 6A



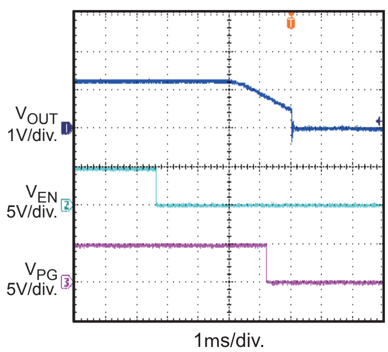
Power Good through V_{IN} Shutdown
I_{OUT} = 6A



Power Good through EN Start-Up
I_{OUT} = 6A



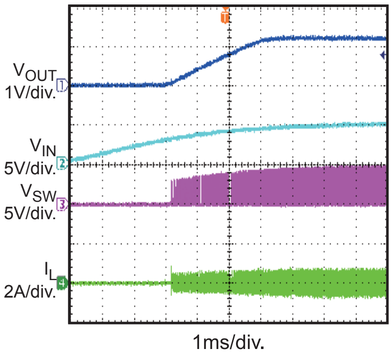
Power Good through EN Shutdown
I_{OUT} = 6A



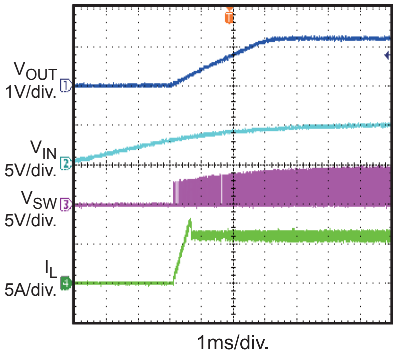
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. MPQ8616GL-6, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

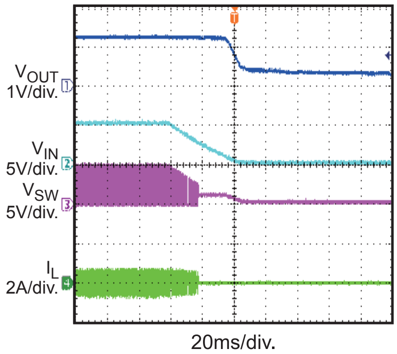
Start-Up through V_{IN}
I_{OUT} = 0A



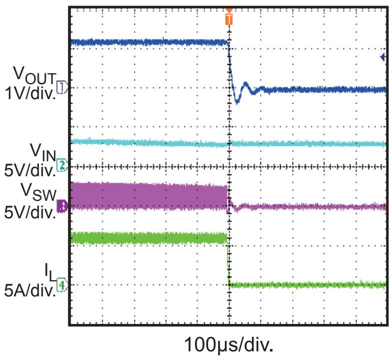
Start-Up through V_{IN}
I_{OUT} = 6A



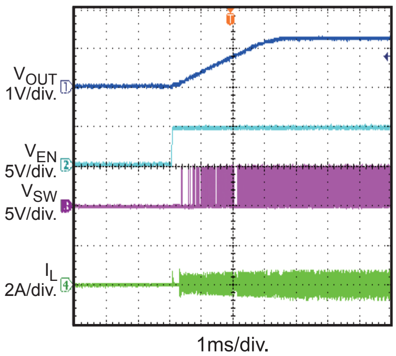
Shutdown through V_{IN}
I_{OUT} = 0A



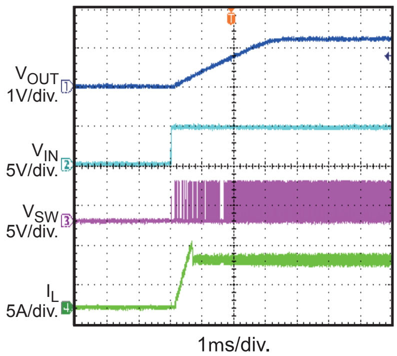
Shutdown through V_{IN}
I_{OUT} = 6A



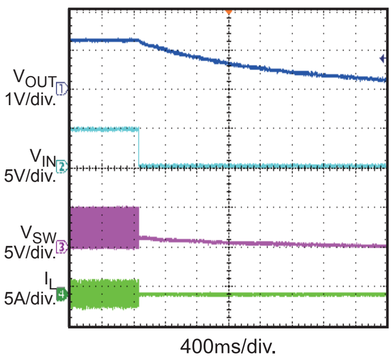
Start-Up through EN
I_{OUT} = 0A



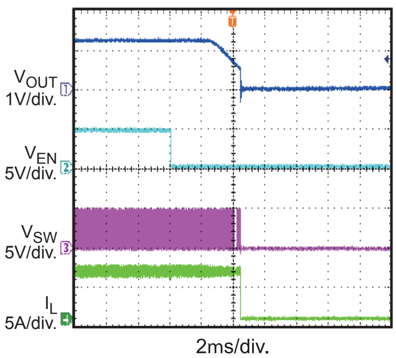
Start-Up through EN
I_{OUT} = 6A



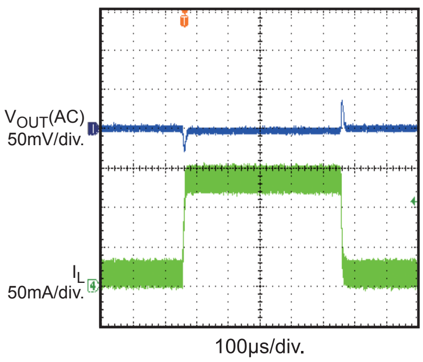
Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
I_{OUT} = 6A



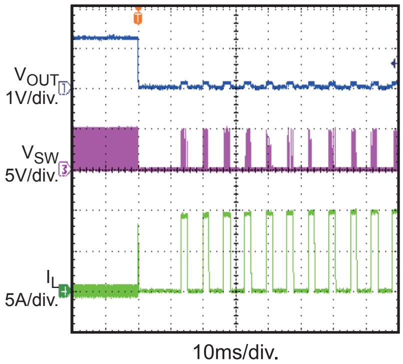
Transient
I_{OUT} = 0.6A-5.4A@2.5A/µs,
f_{SW} = 600kHz, C_{OUT} = 4x22µF



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

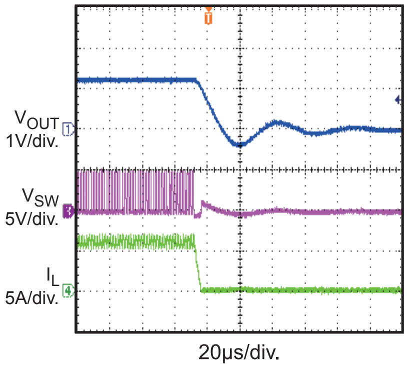
Performance waveforms are tested on the evaluation board of the Design Example section. MPQ8616GL-6, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

Short Circuit Protection



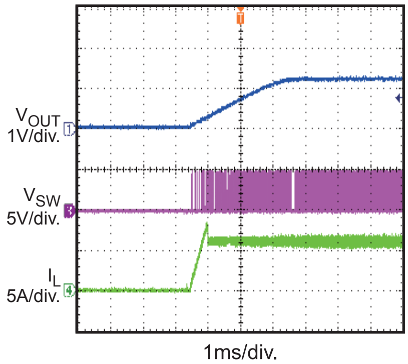
Thermal Shutdown

I_{OUT} = 6A



Thermal Recovery

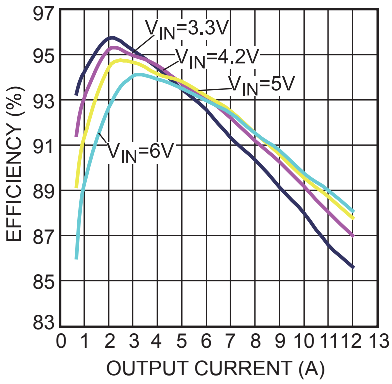
I_{OUT} = 6A



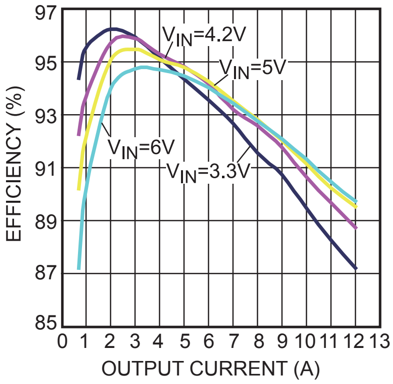
TYPICAL PERFORMANCE CHARACTERISTICS

MPQ8616GL-12, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

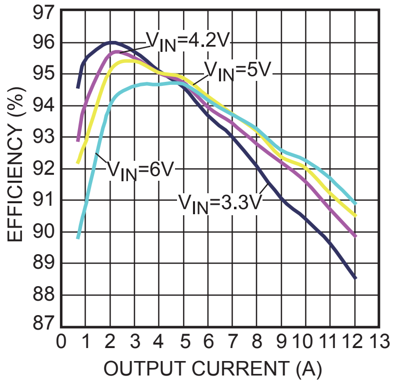
Efficiency
V_{OUT}=1.0V, f_{SW}=600kHz, L=1.0µH



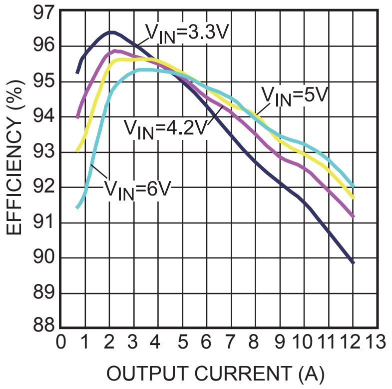
Efficiency
V_{OUT}=1.2V, f_{SW}=600kHz, L=1.0µH



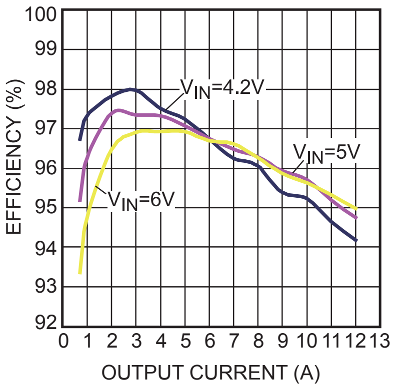
Efficiency
V_{OUT}=1.5V, f_{SW}=600kHz, L=1.0µH



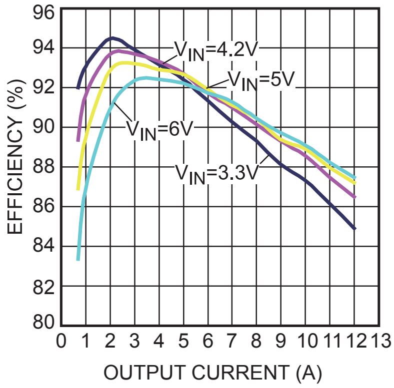
Efficiency
V_{OUT}=1.8V, f_{SW}=600kHz, L=1.0µH



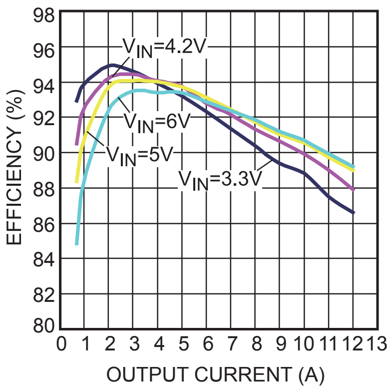
Efficiency
V_{OUT}=3.3V, f_{SW}=600kHz, L=1.0µH



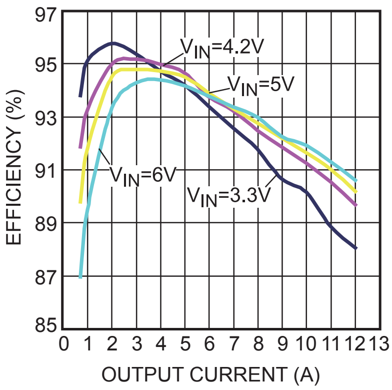
Efficiency
V_{OUT}=1.0V, f_{SW}=800kHz, L=1.0µH



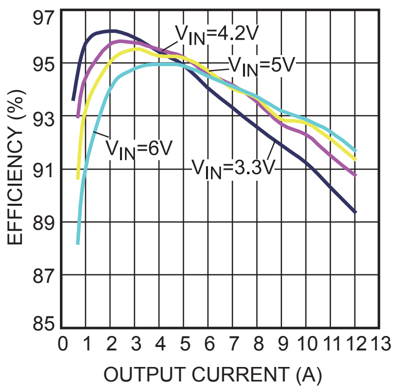
Efficiency
V_{OUT}=1.2V, f_{SW}=800kHz, L=1.0µH



Efficiency
V_{OUT}=1.5V, f_{SW}=800kHz, L=1.0µH



Efficiency
V_{OUT}=1.8V, f_{SW}=800kHz, L=0.82µH

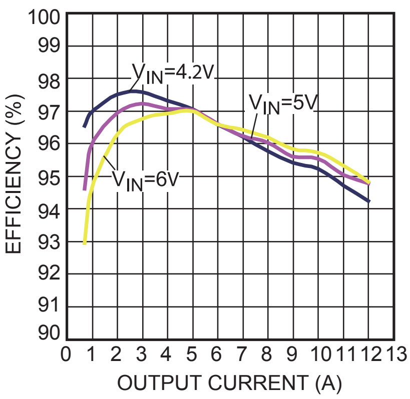


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

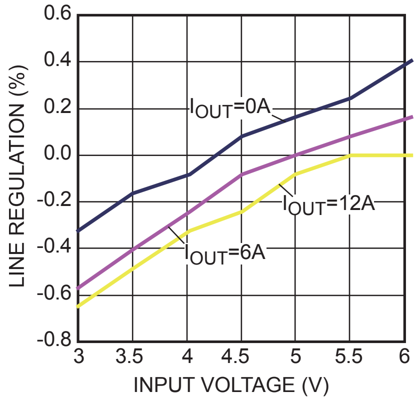
MPQ8616GL-12, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

Efficiency

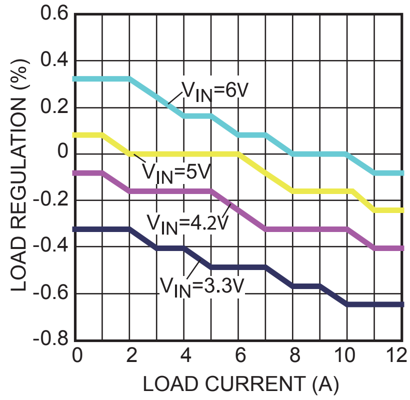
V_{OUT}=3.3V, f_{SW}=800kHz, L=1.0µH



Line Regulation

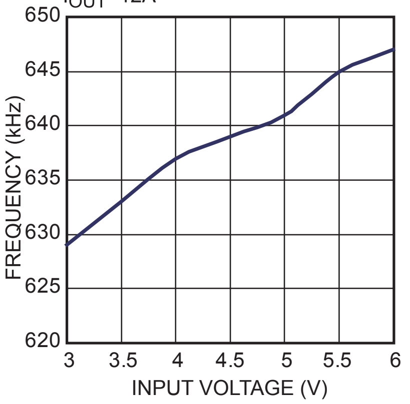


Load Regulation

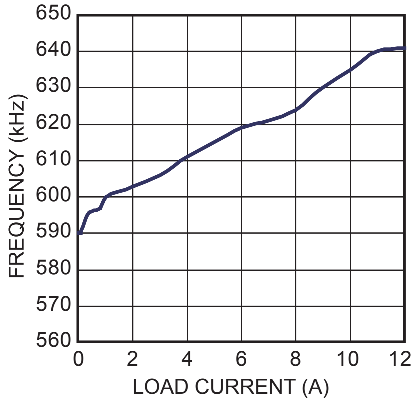


Switching Frequency vs. Input Voltage

I_{OUT}=12A



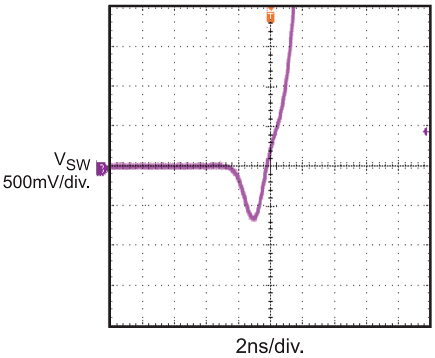
Switching Frequency vs. Load Current



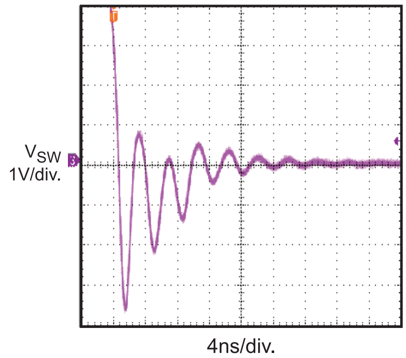
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8616GL-12, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

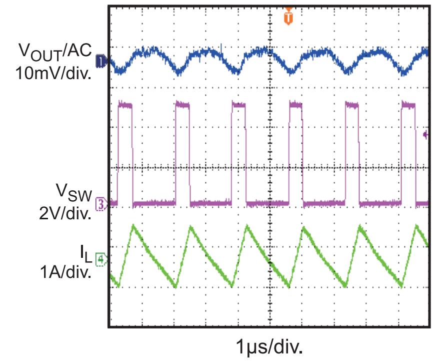
Dead Time On
I_{OUT} = 12A



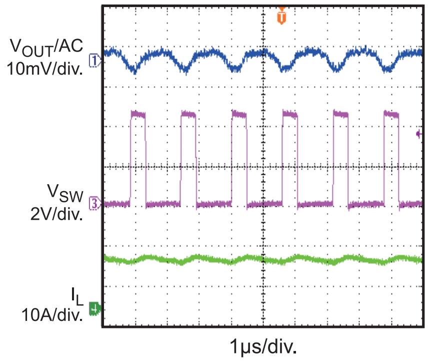
Dead Time Off
I_{OUT} = 12A



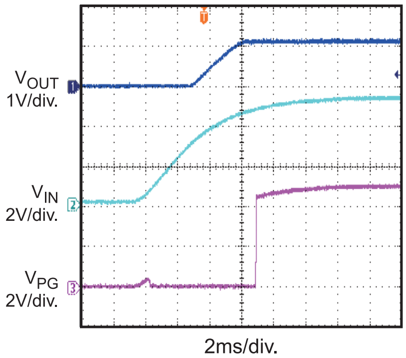
Output Voltage Ripple
I_{OUT} = 0A



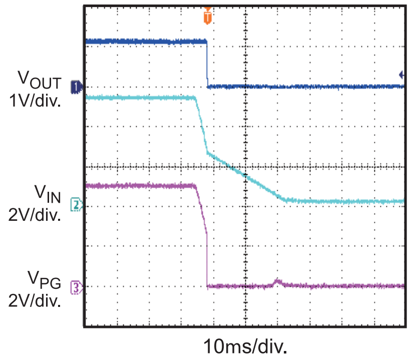
Output Voltage Ripple
I_{OUT} = 12A



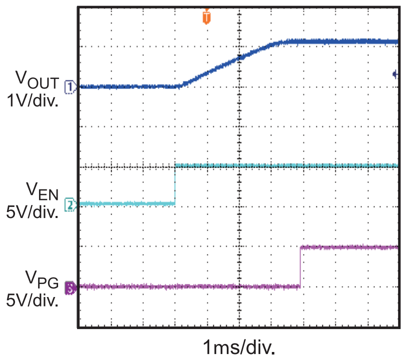
Power Good Through V_{IN} Start-Up
I_{OUT} = 12A



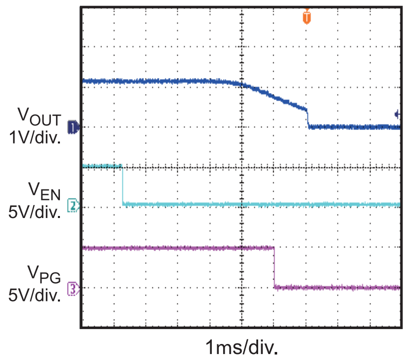
Power Good Through V_{IN} Shutdown
I_{OUT} = 12A



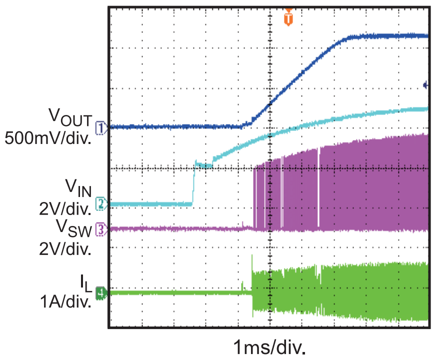
Power Good Through EN Start-Up
I_{OUT} = 12A



Power Good Through EN Shutdown
I_{OUT} = 12A



Start-Up Through V_{IN}
I_{OUT} = 0A

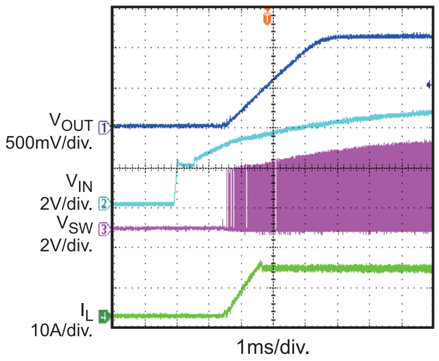


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8616GL-12, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

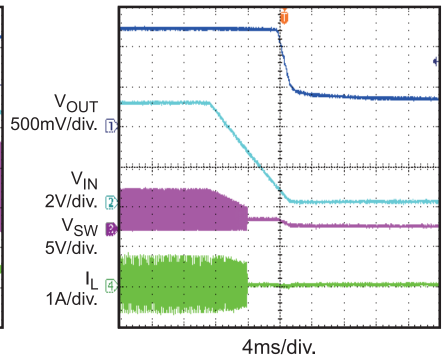
Start-Up Through V_{IN}

I_{OUT} = 12A



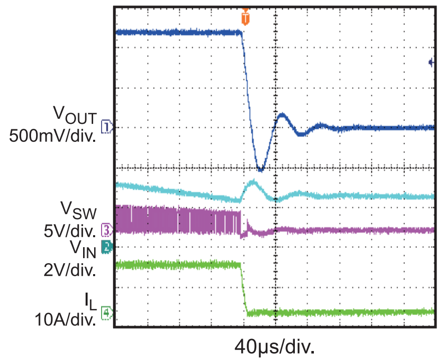
Shutdown Through V_{IN}

I_{OUT} = 0A



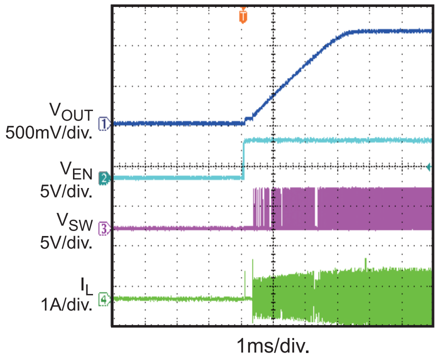
Shutdown Through V_{IN}

I_{OUT} = 12A



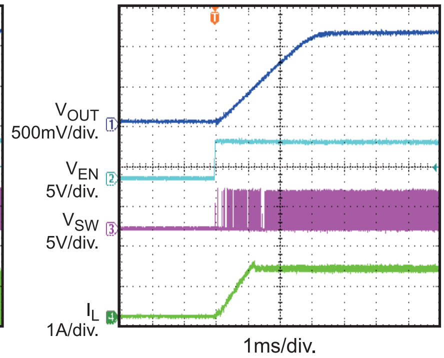
Start-Up Through EN

I_{OUT} = 0A



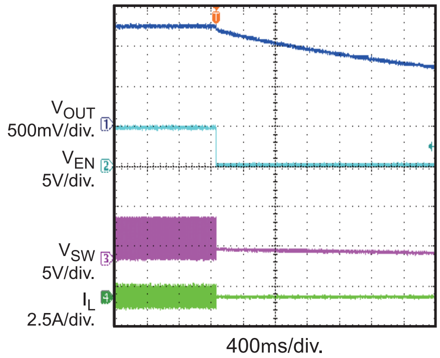
Start-Up Through EN

I_{OUT} = 12A



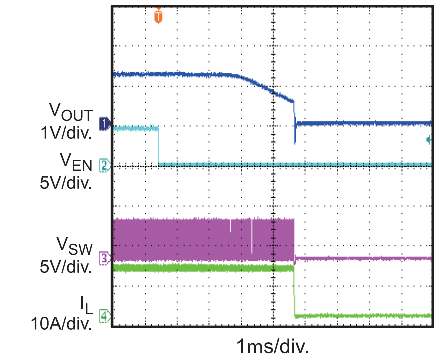
Shutdown Through EN

I_{OUT} = 0A



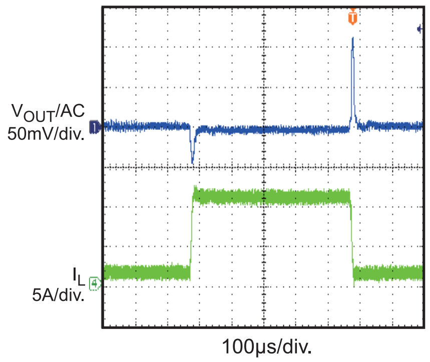
Shutdown Through EN

I_{OUT} = 12A

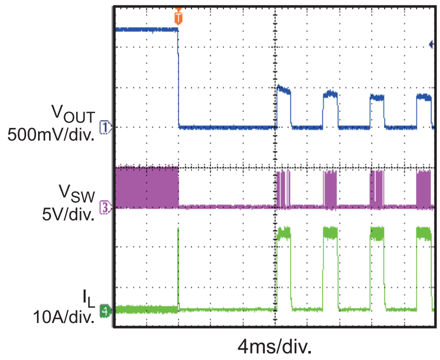


Transient

I_{OUT}=1.2A-10.8A@2.5A/µs,
f_{SW}=600kHz,C_{OUT}=4x22µF



Short Circuit Protection

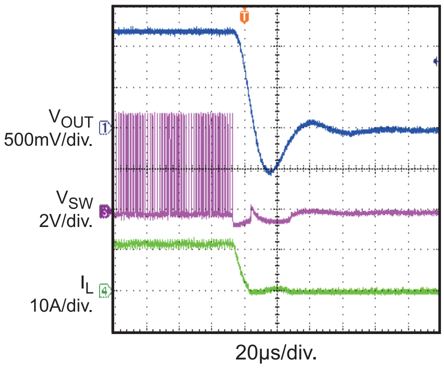


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPQ8616GL-12, V_{IN}=5V, V_{OUT}=1.2V, L=1.0µH, T_A=+25°C, unless otherwise noted.

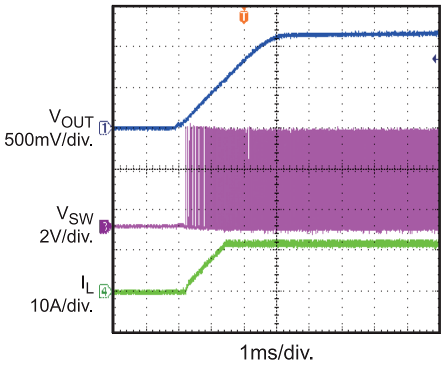
Thermal Shutdown

I_{OUT} = 12A



Thermal Recovery

I_{OUT} = 12A



PIN FUNCTIONS

MPQ8616GL-6, MPQ8616GL-12

PIN #	Name	Description
1	AGND	Analog ground.
2	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. It is recommended to place the resistor divider as close to FB pin as possible. Vias should be avoided on the FB traces.
3	SS	Soft Start. Connect on external capacitor to program the soft start time for the switch mode regulator.
4	EN	Enable pin. Pull this pin higher than 1.8V to enable the chip. For automatic start-up, connect EN pin to VIN with 100KΩ resistor. Can be used to set the on/off threshold (adjust UVLO) with two additional resistors. When the nominal VOUT is higher than 2.5V, EN should be pulled low before VIN powers off.
5	VCC	External bias supply voltage for driver and control circuits. For 1.5V to 3V input application, provide VCC with separate 3.3V/5V bias supply. For 3V to 6V input application, provide VCC with separate 3.3V/5V bias supply or tie VCC to VIN with 10ohm resistor. Decouple with a minimum 4.7µF ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
6	PG	Power good output. It is high if the output voltage is higher than 90% of the nominal voltage. There is a delay from FB ≥ 90% to PG goes high.
7	BST	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
8-9	GND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout.
10-11	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MPQ8616 operate from a +3V to +6V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
12	FREQ	Frequency setting pin. A resistor connected between FREQ and IN is required to set the switching frequency. The ON time is determined by the input voltage and the resistor connected to the FREQ pin. IN connect through a resistor is used for line feed-forward and makes the frequency basically constant during input voltage's variation. Recommend a 10pF decoupling capacitor from FREQ to GND.
13-14	SW	Switch Output. Connect this pin to the inductor and bootstrap capacitor. This pin is driven up to the VIN voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives the SW pin negative during the off-time. The on-resistance of the low-side switch and the internal Schottky diode fixes the negative voltage. Use wide PCB traces to make the connection.

BLOCK DIAGRAM

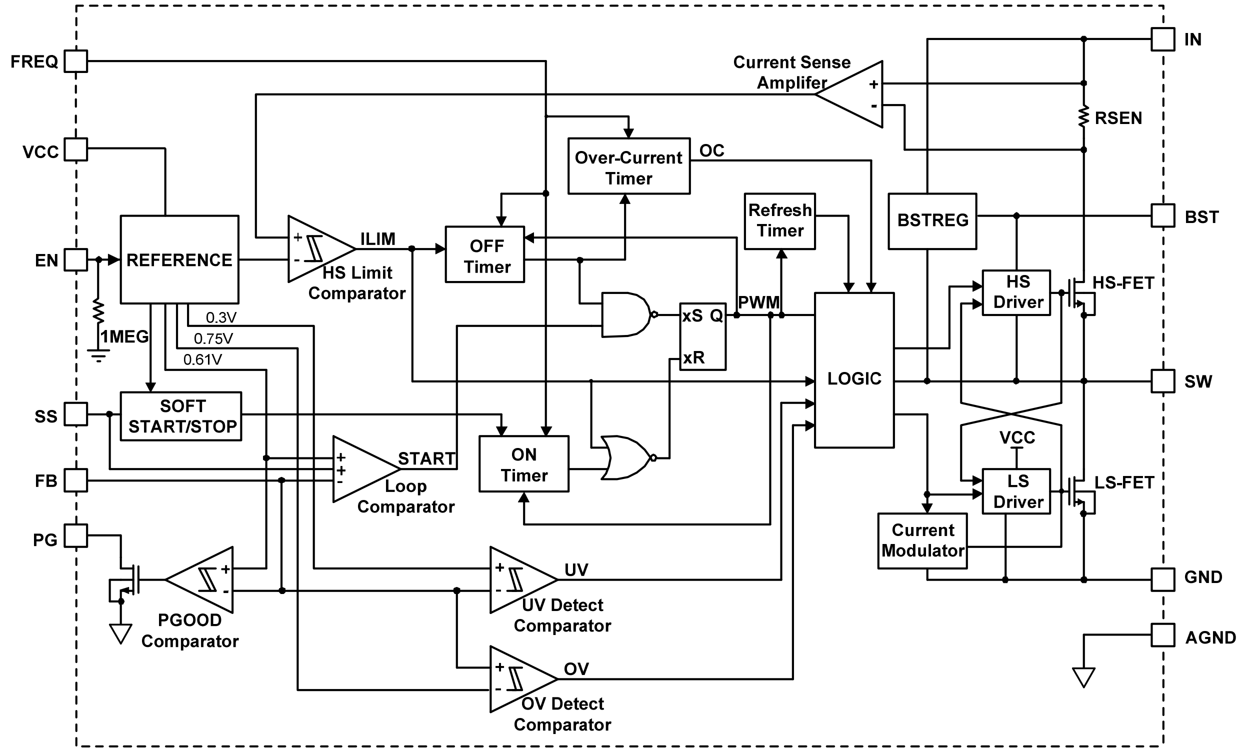


Figure 1—Functional Block Diagram

OPERATION

PWM Operation

The MPQ8616 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The ON period is determined by the input voltage and the frequency-set resistor as follows:

$$t_{ON}(ns) = \frac{4.8 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.49} \quad (1)$$

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS-FET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

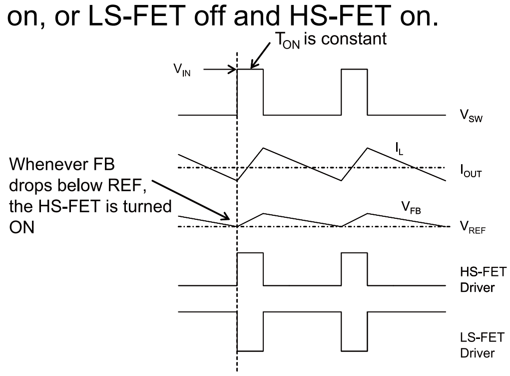


Figure 2—PWM Operation

MPQ8616 always operating in continuous-conduction-mode (CCM), which means the inductor current can go negative at light load. The CCM mode operation is shown in Figure2. When V_{FB} is below V_{REF}, HS-MOSFET is turned on for a fixed interval which is determined by one- shot on-timer as equation 1 shown. When the HS-MOSFET is turned off, the LS-MOSFET is turned on until next period.

For the MPQ8616 is operated in CCM, the switching frequency is fairly constant and it is called PWM mode.

Switching Frequency

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and capacitance to maintain low output voltage ripple.

For MPQ8616, the on time can be set using FREQ pin, then the frequency is set in steady state operation at CCM mode.

Adaptive constant-on-time (COT) control is used in MPQ8616 and there is no dedicated oscillator in the IC. Connect FREQ pin to IN pin through resistor R_{FREQ} and the input voltage is feed-forwarded to the one-shot on-time timer through the resistor R_{FREQ}. When in steady state operation at CCM, the duty ratio is kept as V_{OUT}/V_{IN}. Hence the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as follows:

$$f_{SW}(kHz) = \frac{10^6}{\frac{4.8 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.49} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + t_{DELAY}(ns)} \quad (2)$$

Where t_{DELAY} is the comparator delay. It's about 40ns.

Generally, the MPQ8616 is set for 300kHz to 1MHz application. It is optimized to operate at high switching frequency with high efficiency. High switching frequency makes it possible to utilize small sized LC filter components to save system PCB space.

Jitter and FB Ramp Slope

Figure 3 shows jitter occurring in PWM mode. When there is noise in the V_{FB} downward slope, the ON time of HS-FET deviates from its intended location and produces jitter. It is necessary to understand that there is a relationship between a system's stability and the steepness of the V_{FB} ripple's downward slope. The slope steepness of the V_{FB} ripple dominates in noise immunity. The magnitude of the V_{FB} ripple doesn't affect the noise immunity directly.

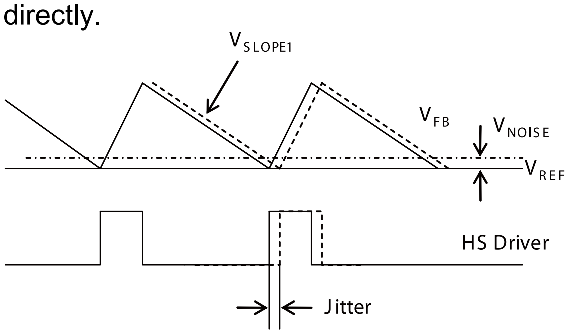


Figure 3—Jitter in PWM Mode

Ramp with Large ESR Capacitor

In the case of POSCAP or other types of capacitor with lager ESR is applied as output capacitor, the ESR ripple dominates the output ripple, and the slope on the FB is quite ESR related. Figure 4 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. Turn to application information section for design steps with large ESR capacitors.

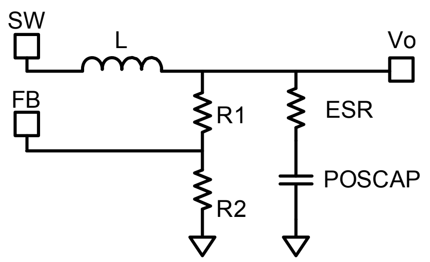


Figure 4—Simplified Circuit in PWM Mode without External Ramp Compensation

To realize the stability when no external ramp is applied, usually the ESR value should be chosen as follow:

$$R_{ESR} \ge \frac{\frac{t_{SW}}{0.7\times\pi} + \frac{t_{ON}}{2}}{C_{OUT}} \quad (3)$$

T_{SW} is the switching period.

Ramp with Small ESR Capacitor

When the output capacitors are ceramic ones, the ESR ripple is not high enough to stabilize the system, and external ramp compensation is needed. Skip to application information section for design steps with small ESR caps.

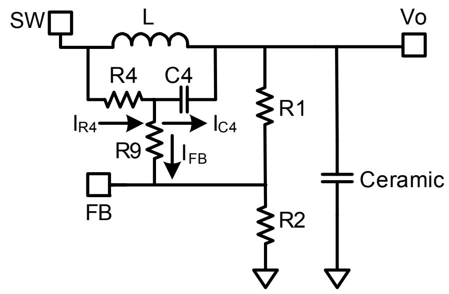


Figure 5—Simplified Circuit in PWM Mode with External Ramp Compensation

In PWM mode, an equivalent circuit with HS-FET off and the use of an external ramp compensation circuit (R4, C4) is simplified in Figure 5. The external ramp is derived from the inductor ripple current. If one chooses C4, R9, R1 and R2 to meet the following condition:

$$\frac{1}{2\pi\times f_{SW}\times C_4} < \frac{1}{20}\times\left(\frac{R_1\times R_2}{R_1+R_2}+R_9\right) \quad (4)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (5)$$

And the ramp on the V_{FB} can then be estimated as:

$$V_{RAMP} = \frac{V_{IN}-V_O}{R_4\times C_4}\times t_{ON}\times\left(\frac{R_1 // R_2}{R_1 // R_2 + R_9}\right) \quad (6)$$

The downward slope of the V_{FB} ripple then follows:

$$V_{SLOPE1} = \frac{V_{RAMP}}{t_{off}} = \frac{-V_{OUT}}{R_4\times C_4} \quad (7)$$

As can be seen from equation 7, if there is instability in PWM mode, we can reduce either R4 or C4. If C4 can not be reduced further due to limitation from equation 4, then we can only reduce R4. For a stable PWM operation, the V_{slope1} should be design follow equation 8.

$$-V_{SLOPE1} \ge \frac{\frac{t_{SW}}{0.7\times\pi}+\frac{t_{ON}}{2}-R_{ESR}\times C_{OUT}}{2\times L\times C_{OUT}}\times V_{OUT} + \frac{0.7\times I_O\times 10^{-3}}{t_{sw}-t_{on}} \quad (8)$$

Where Io is the load current.

Soft Start/Stop

The MPQ8616 employs soft start/stop (SS) mechanism to ensure smooth output during power up and power down.

When the EN pin becomes high, an internal current source (8μA) charges up the SS capacitor C6. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it keeps ramping up while V_{REF} takes over the PWM comparator. At this point, the soft start finishes and it enters into steady state operation.

When the EN pin is pulled to low, the SS CAP voltage is discharged through an 8uA internal current source. Once the SS voltage reaches REF voltage, it takes over the PWM comparator. The output voltage will decrease smoothly with SS voltage until zero level. The SS capacitor value can be determined as follows:

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}} \quad (9)$$

If the output capacitors have large capacitance value, it's not recommended to set the SS time too small. Otherwise, it's easy to hit the current limit during SS. A minimum value of 4.7nF should be used if the output capacitance value is larger than 330μF.

Pre-Bias Startup

If the output is pre-biased to a certain voltage during startup, the MPQ8616 will disable the switching of both high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the sensed output voltage at the FB pin.

Power Good (PG)

The MPQ8616 has power-good (PG) output. It can be connected to V_{CC} or other voltage source through a resistor (e.g. 100k). When the MPQ8616 is powered on and FB voltage reaches above 90% of REF voltage, the PG pin is pulled high.

When the FB voltage drops to 70% of REF voltage or the part is not powered on, the PG pin will be pulled low.

Over-Current Protection (OCP)

The MPQ8616 enters over-current protection mode when the inductor current hits the current limit, and tries to recover from over-current fault with hiccup mode. That means in over-current protection, the chip will disable output power stage, discharge soft-start capacitor and then automatically try to soft-start again. If the over-current condition still holds after soft-start ends, the chip repeats this operation cycle till over-current disappears and output rises back to regulation level. The MPQ8616 also operates in hiccup mode when short circuit happens.

Over/Under –Voltage Protection (OVP/UVP)

The MPQ8616 has non-latching over voltage protection. It monitors the output voltage through a resistor divider feedback (FB) voltage to detect over-voltage on the output. When the FB voltage is higher than 120% of the REF voltage (0.610V), the LS-FET will be turned on while the HS-FET will be off. The LS-FET keeps on until it hits the negative current limit and turns off for 100ns. If over voltage condition still holds, the chip repeats this operation cycle till the FB voltage drops below 110% of the REF voltage.

When the FB voltage is below 50% of the REF voltage (0.610V), it is recognized as under-voltage (UV). Usually, UVP accompanies a hit in current limit and results in OCP.

Configuring the EN Control

The EN pin provides electrical on/off control of the device. Set EN high to turn on the regulator and low to turn it off. Do not float this pin.

For automatic start-up, the EN pin can be pulled up to input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from VIN pin to EN pin) and the pull-down resistor (R_{DOWN} from EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.4 \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (10)$$

For example, for R_{UP} =100kΩ and R_{DOWN} =51kΩ, the $V_{IN-START}$ is set at 4.15V.

To avoid noise, a 10nF ceramic capacitor from EN to GND is recommended.

There is an internal zener diode on the EN pin, which clamps the EN pin voltage to prevent it from running away. The maximum pull up current assuming a worst case 6V internal zener clamp should be less than 1mA. Therefore, when EN is driven by an external logic signal, the EN voltage should be lower than 6V; when EN is connected with VIN through a pull-up resistor or a resistive voltage divider, the resistance selection should ensure the maximum pull up current less than 1mA.

If using a resistive voltage divider and VIN higher than 6V, the allowed minimum pull-up resistor R_{UP} should meet the following equation:

$$\frac{V_{IN}(V)-6}{R_{UP}(k\Omega)}-\frac{6}{R_{DOWN}(k\Omega)}<1(mA) \quad (11)$$

As a result, when just the pull-up resistor R_{UP} is applied, the $V_{IN-START}$ is determined by input UVLO. The value of R_{UP} can be got as:

$$R_{UP}(k\Omega)>\frac{V_{IN}(V)-6}{1(mA)} \quad (12)$$

A typical pull-up resistor is 100kΩ.

When the nominal VOUT is higher than 2.5V, to avoid the converter operation with minimum off time during power off, EN should be pulled low before VIN powers off. Figure 6 shows the recommended power off sequence.

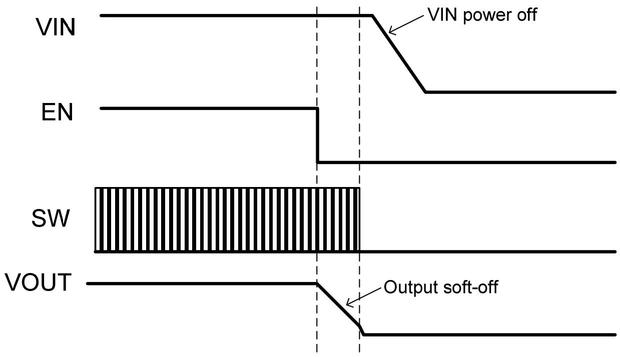


Figure 6 —Power Off Sequence when VOUT > 2.5V

UVLO protection

The MPQ8616 has under-voltage lock-out protection (UVLO). When the VCC voltage is higher than the UVLO rising threshold voltage, the MPQ8616 will be powered up. It shuts off when the VCC voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.The MPQ8616 is disabled when the VCC voltage falls below its UVLO falling threshold (2.45V). If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 7 to adjust the input voltage UVLO by using two external resistors. It is recommended to use the enable resistors to set the UVLO falling threshold (V_{STOP}) above 2.8 V. The rising threshold (V_{START}) should be set to provide enough hysteresis to allow for any input supply variations.

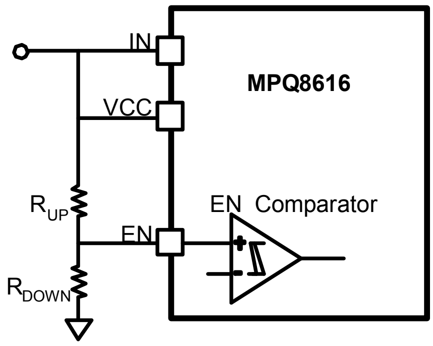


Figure 7—Adjustable UVLO

When the nominal VOUT is higher than 2.5V, EN should be pulled low before VIN powers off.

Thermal Shutdown

Thermal shutdown is employed in the MPQ8616. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (minimum 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a soft startup.

APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Caps

For applications that electrolytic capacitor or POS capacitor with a controlled output of ESR is set as output capacitors. The output voltage is set by feedback resistors R1 and R2. As figure 8 shows.

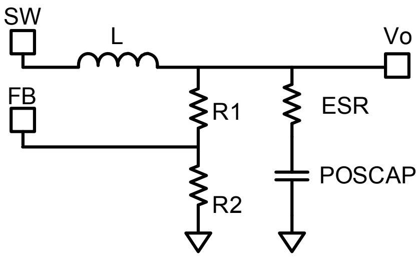


Figure8—Simplified Circuit of POS Capacitor

First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-100kΩ for R2, using a comparatively larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. Then R1 is determined as follow with the output ripple considered:

$$R_1 = \frac{V_{OUT} - \frac{1}{2} \times \Delta V_{OUT} - V_{REF}}{V_{REF}} \times R_2 \quad (13)$$

ΔV_{OUT} is the output ripple determined by equation 21.

Setting the Output Voltage-Small ESR Caps

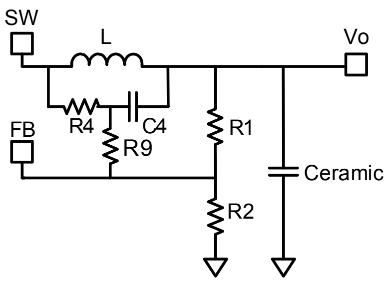


Figure9—Simplified Circuit of Ceramic Capacitor

When low ESR ceramic capacitor is used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4.The output voltage is influenced by ramp voltage V_{RAMP} besides resistor divider as shown in Figure 9. The V_{RAMP} can be calculated as shown in equation 6. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-100kΩ for R2, using a comparatively larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. And the value of R1 then is determined as follow:

$$R_1 = \frac{R_2}{\frac{V_{FB(AVG)}}{V_{OUT} - V_{FB(AVG)}} - \frac{R_2}{R_4 + R_9}} \quad (14)$$

The $V_{FB(AVG)}$ is the average value on the FB. $V_{FB(AVG)}$ varies with the Vin, Vo, and load condition, etc.. It is means the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$,if one wants to gets a better load or line regulation, a lower V_{RAMP} is suggested once it meets equation 8.

For PWM operation, $V_{FB(AVG)}$ value can be deduced from equation 15.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} \times V_{RAMP} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (15)$$

Usually, R9 is set to 0Ω, and it can also be set following equation 16 for a better noise immunity. It should be set to be 5 timers smaller than R1//R2 to minimize its influence on Vramp.

$$R_9 \le \frac{1}{10} \times \frac{R_1 \times R_2}{R_1 + R_2} \quad (16)$$

Using equation 14 and 15 to calculate the output voltage can be complicated. To simplify the calculation of R1 in equation 14, a DC-blocking capacitor Cdc can be added to filter the DC influence from R4 and R9. Figure 9 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using equation 17 for PWM mode operation.

$$R_1 = \frac{V_{OUT} - V_{REF} - \frac{1}{2} \times V_{RAMP}}{V_{REF} + \frac{1}{2} \times V_{RAMP}} \times R_2 \quad (17)$$

Cdc is suggested to be at least 10 times larger than C4 for better DC blocking performance, and should be not larger than 0.47μF considering startup performance. In case one wants to use larger Cdc for a better FB noise immunity, combined with reduced R1 and R2 to limit the Cdc in a reasonable value without affecting the system start up. Be noted that even when the Cdc is applied, the load and line regulation are still Vramp related.

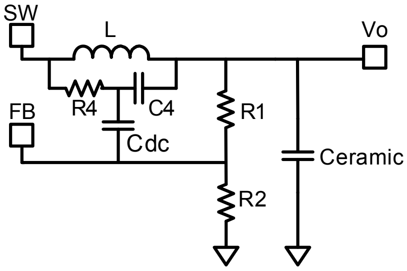


Figure10—Simplified Circuit of Ceramic Capacitor with DC blocking capacitor

Input Capacitor

The input current to the step-down converter is discontinuous. Therefore, a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance. In the layout, it's recommended to put the input capacitors as close to the IN pin as possible.

The capacitance varies significantly over temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over temperature.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (18)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (19)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is input voltage ripple requirement in the system design, choose the input capacitor that meets the specification

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (20)$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (21)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (22)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (23)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4 following equation 4, 7 and 8.

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value according to equation 3 is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (24)$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switching input voltage. A larger value inductor will result in less ripple current and lower output ripple voltage. However, a larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductor value is to allow the peak-to-peak ripple current in the inductor to be approximately 10~30% of the maximum output current. Also, make sure that the peak inductor current is below the current limit of the device. The inductance value can be calculated as:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (25)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (26)$$

The inductors listed in Table 1 are highly recommended for the high efficiency they can provide.

Table 1—Inductor Selection Guide

Part Number	Manufacturer	Inductance (µH)	DCR (mΩ)	Current Rating (A)	Dimensions L x W x H (mm³)	Switching Frequency (kHz)
FDU1250C-R50M	TOKO	0.50	1.3	46.3	13.3 x 12.1 x5	1000
FDU1250C-R56M	TOKO	0.56	1.6	42.6	13.3 x 12.1 x5	800-1000
FDU1250C-R75M	TOKO	0.75	1.7	32.7	13.3 x 12.1 x5	600-800
FDU1250C-1R0M	TOKO	1.0	2.2	31.3	13.3 x 12.1 x5	600

Typical Design Parameter Tables

The following tables include recommended component values for typical output voltages (1.0V, 1.2V, 1.8V, 3.3V) and switching frequencies (600kHz, 800kHz, and 1MHz). Refer to Tables 2-4 for design cases without external ramp compensation and Tables 5-6 for design cases with external ramp compensation. External ramp is not needed when high-ESR capacitors, such as electrolytic or POSCAPs are used. External ramp is needed when low-ESR capacitors, such as ceramic capacitors are used. For cases not listed in this datasheet, a calculator in excel spreadsheet can also be requested through a local sales representative to assist with the calculation.

Table 2—C_{OUT}-Poscap, 600kHz, 5V_{IN}

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.0	1.0	19.8	30	300
1.2	1.0	29.4	30	365
1.5	1.0	29.4	20	453
1.8	1.0	39.2	20	549
3.3	1.0	44.2	10	1000

Table 3—C_{OUT}-Poscap, 800kHz, 5VIN

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.0	0.75	20	30	210
1.2	0.75	20	20	270
1.5	0.75	30	20	330
1.8	0.75	39	20	499
3.3	0.75	44.2	10	750

Table 5—C_{OUT}-Ceramic, 600kHz, 5VIN

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.0	1.0	21	30	240	470	309
1.2	1.0	33	30	220	470	365
1.5	1.0	51	30	330	390	464
1.8	1.0	45	20	270	470	549
3.3	1.0	62	10	160	680	953

Table 6—C_{OUT}-Ceramic, 800kHz, 5VIN

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.0	0.75	21	30	200	470	226
1.2	0.75	34	30	200	470	270
1.5	0.75	34	20	220	470	324
1.8	0.75	47.5	20	225	470	402
3.3	0.75	57.6	10	200	560	750

TYPICAL APPLICATION

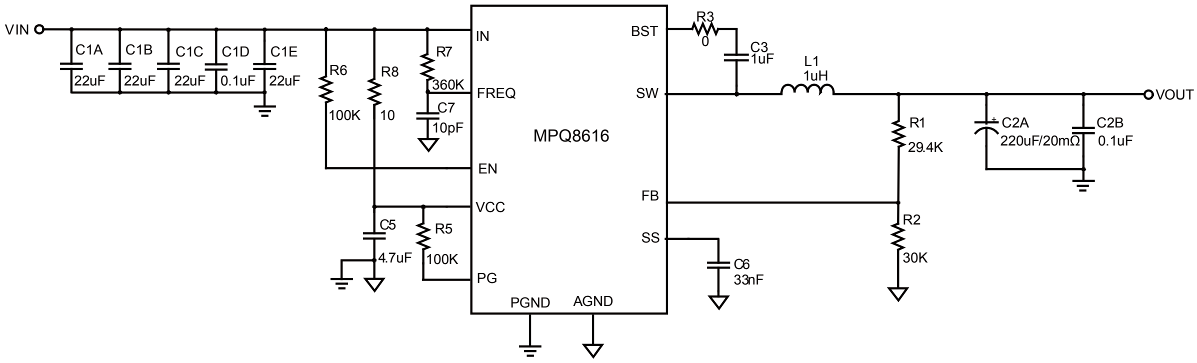


Figure 13 — Typical Application Circuit with No External Ramp

MPQ8616, V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=6/12A, f_{SW}=600kHz

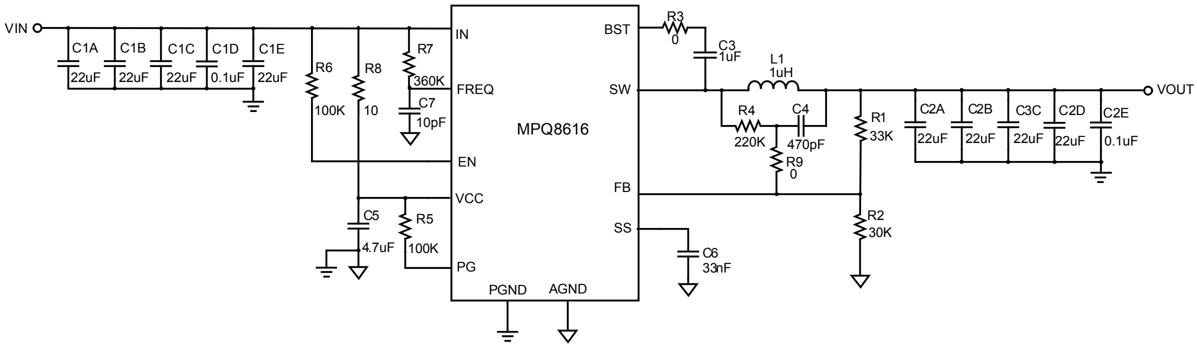


Figure 14 — Typical Application Circuit with Low ESR Ceramic Capacitor

MPQ8616, V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=6/12A, f_{SW}=600kHz

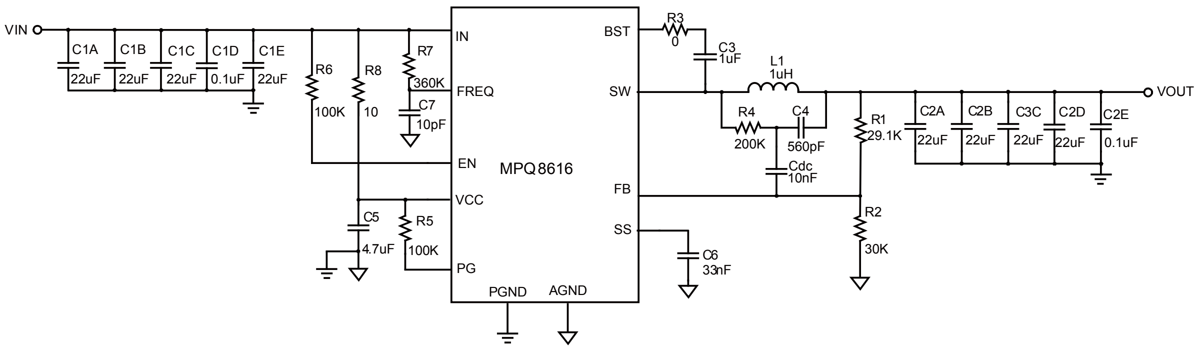


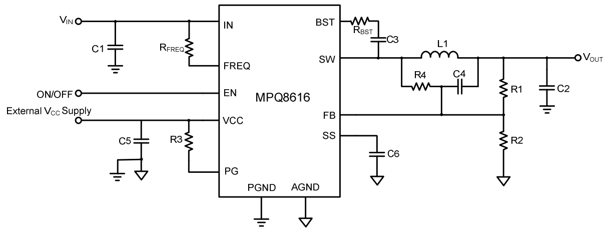
Figure 15 — Typical Application Circuit with Low ESR Ceramic Capacitor

and DC-Blocking Capacitor.

MPQ8616, V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=6/12A, f_{SW}=600kHz

LAYOUT RECOMMENDATION

1. Four-layer layout is strongly recommended to achieve better thermal performance.
2. Place at least 9 vias (10/20mil hole/diameter size) right beneath the IC to get best decoupling effect.
3. Place 10 or more vias (10/25mil hole/diameter size) each for input and GND copper next to the VIN and PGND pin to improve the thermal performance.
4. A 22uF (1206/1210) input cap C1B is required on bottom layer, right beneath the VIN/PGND vias to get best input decoupling effect.
5. If VIN/PGND vias is not allowed beneath the IC, a 22uF input cap with 1206/1210 package (C1C) is required on the Top layer as Figure17, connecting to VIN and PGND copper directly, within 2mm of the IC edge.
6. A solid PGND layer is required to place on the first inner layer, right below the IC layer.
7. The high current paths (GND, IN, and SW) should be placed very close to the device with short, direct and wide traces.
8. VCC decoupling capacitor (C5) should be as close to the VCC pin as possible, connect its GND net to PGND copper.
9. Connect all AGND signals together to AGND pin at first, then Kelvin connect AGND to PGND near the VCC decoupling capacitor(C5) GND pad on Top layer. Keep AGND trace 20mil or wider.
10. The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace and away from the switching node SW.
11. Keep the BST voltage path (BST, C3, Rbst and SW) as short as possible.
12. Keep the Vout sense trace away from noise signal, such as SW, VIN, etc. Put the Vout sense point to a stable, quiet output point close to Vout cap.



Schematic for PCB Layout Guide Line

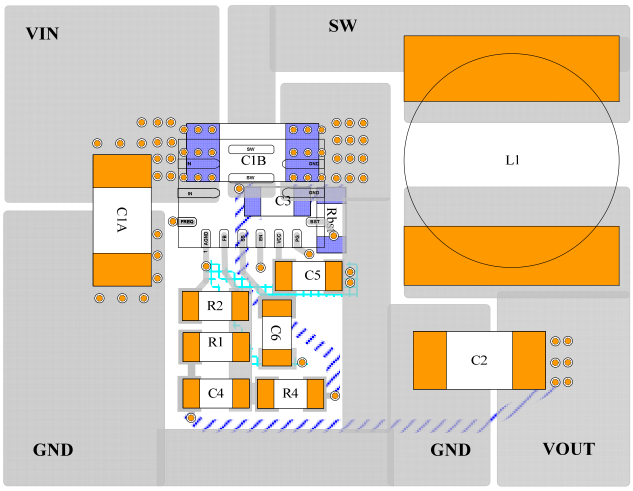


Figure 16—PCB LAYOUT

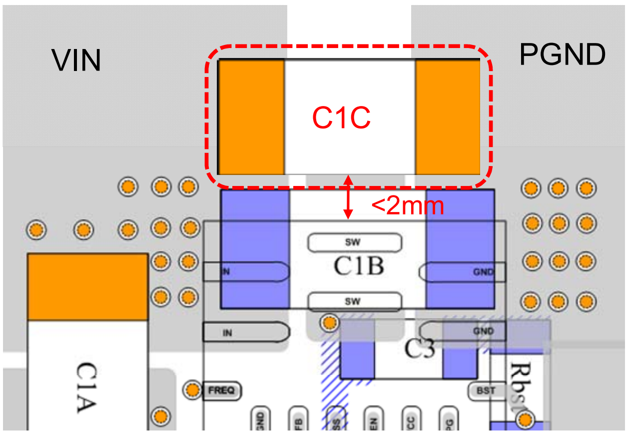
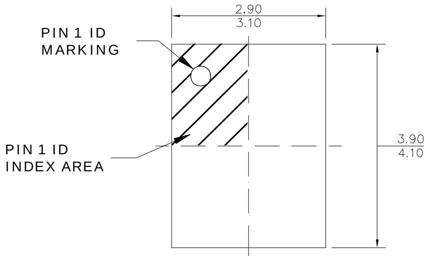


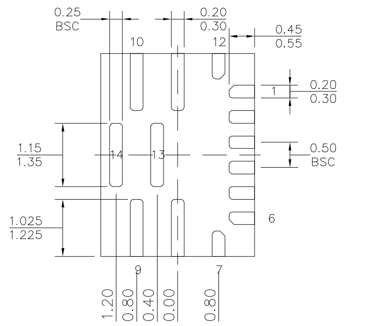
Figure 17—VIN Decouple Capacitor

PACKAGE INFORMATION

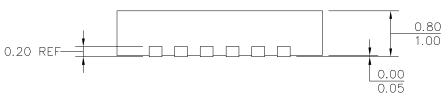
QFN (3mmx4mm)



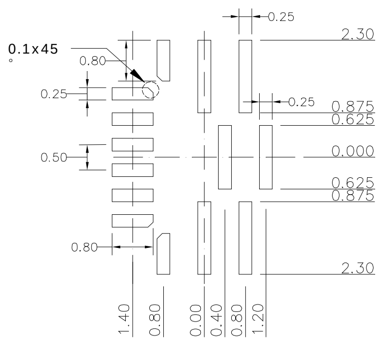
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.