PAC7640: Enhanced QE Global Shutter Image Sensor

General Description

PAC7640 is a global shutter image sensor with enhanced Quantum Efficiency (QE) in the NIR region. PAC7640 is well suited for applications where conservation of NIR LED power is critical. It features 400x400 resolution with image capture capability of 120 frame per second (fps) at full resolution.

The sensor comes with an integrated image sensor ISP. In addition, the PAC7640 also allows for multiple camera synchronization, which makes it suitable for 3D stereo type applications. All ISP functionalities can be controlled through register settings via I^2C.

Key Features

- Ultra-low power consumption
- Enhanced QE in NIR region
- FSYNC signal to synchronize sensors
- Data format: Full 8/10 bit RAW
- MIPI CSI2 for data interface
- Programmable MIPI virtual channels
- I^2C with speed up to 400 kbit/s as control interface
- Configurable LED Pulse width
- Register programmable device ID
- Image Signal Processing (ISP) features
- Lens distortion correction (LDC)
- Lens shading correction (LSC)
- Auto Exposure and Gain Control
- Intensity Histogram

Applications

- 3D Stereo type mapping
- Gesture recognition
- Face recognition

Key Parameters

Parameter	Value
Array Size (pixels)	400 x 400
Pixel Size (µm)	3.0 x 3.0
Shutter Type	Electronic global shutter
Max Frame Rate (fps)	120 at full resolution
Signal to Noise Ratio, SNR (dB)	38.8
Dynamic Range (dB)	51.4
Sensitivity (V/Lux-sec)	7.5 @ 3100K
Quantum Efficiency (%)	40.0 (at 850 nm) 18.2 (at 940 nm)
Input Clock (MHz)	9.6, 14/12.8/19.2
Supply Voltage (V)	Analog: 2.8V Digital: 1.5V I/O: 1.8V
Power Consumption	65 mW @ 120fps 2.7 mW @ Standby 15 uW @ Sleep mode
Operating Temperature, T_j (°C)	-20 to +70
Package Type	Chip Scale Package (CSP)
Package Dimension (mm)	3.42 x 3.42 x 0.76

Ordering Information

Part Number	Description
PAC7640LT	36-balls CSP. Available in Tray packing.

Lead (Pb) Free RoHS 6 fully compliant

For any additional inquiries, please contact us at http://www.pixart.com/contact.asp.

Contents

1.0 Introduction

1.1 System Overview

The PAC7640 is based on CMOS image sensor technology. It is designed to meet the increasingly demanding needs for computer vision in 3D Stereo type mapping or mobile devices. Figure 1 illustrates a typical system application diagram. All the image sensing, signal processing, timing synchronization are handled by the PAC7640.

PAC7640 can be configured to produce different frame rate and should the system require multiple camera (through the use of FSYNC), the image output from each camera can be configured to output at a delay to the Host.

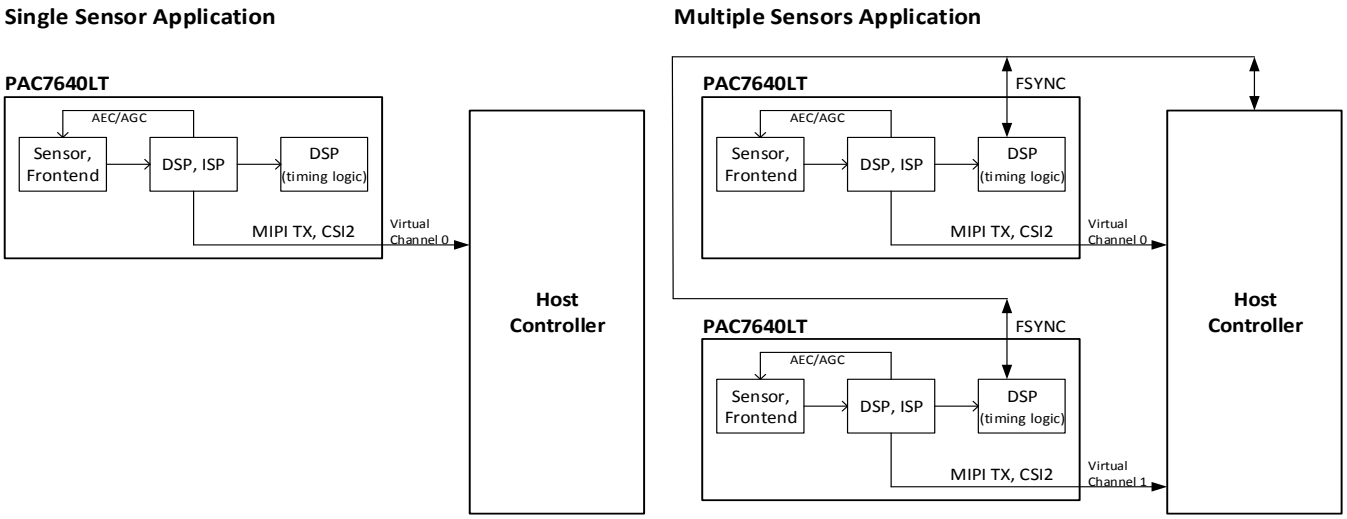

Figure 1. System Overview

1.2 Block Diagram

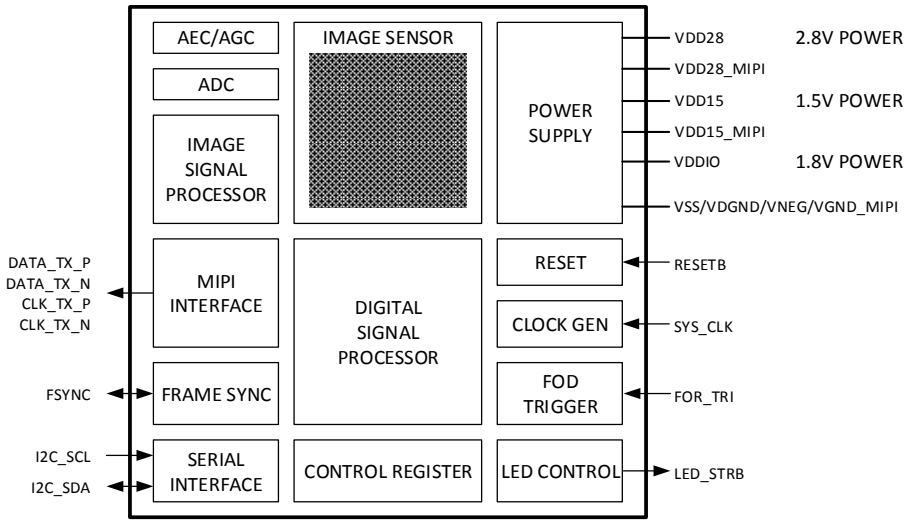

Figure 2. Functional Block Diagram

1.3 Pin Configuration

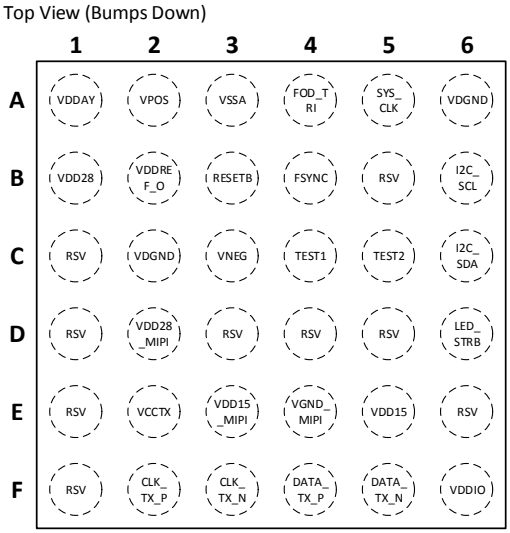

Figure 3. Ball Map Configuration

Table 1. PAC7640LT Pin Description

Pin No.	Symbol	Type	Description
Function	**Power Supplies**		
A1	VDDAY	Output	Regulator output, for sensor power reference. Connect to a 0.1uF bypass capacitor.
A2	VPOS	Output	Regulator output, for sensor power reference. Connect to a 47nF bypass capacitor.
B1	VDD28	Power	2.8 volt analog power supply. Connect to a 0.1uF bypass capacitor.
B2	VDDREF_O	Output	Regulator output, for ADC power reference. Connect to a 0.1uF bypass capacitor.
D2	VDD28_MIPI	Power	2.8 volt MIPI power supply, for LP signal reference. Connect to a 0.1uF bypass capacitor.
E2	VCCTX	Output	Regulator output, for MIPI HS signal reference. Connect to a 0.1uF bypass capacitor.
E3	VDD15_MIPI	Power	1.5 volt MIPI power supply, for HS signal reference. Connect to a 0.1uF bypass capacitor.
E5	VDD15	Power	1.5 volt digital core power supply. Connect to a 0.1uF bypass capacitor.
F6	VDDIO	Power	1.8 volt IO power supply. Connect to a 0.1uF bypass capacitor.
A3	VSSA	Ground	Analog ground.
A6	VDGND	Ground	Digital core ground.
C2	VDGND	Ground	Digital core ground.
C3	VNEG	Ground	Sensor ground.
E4	VGND_MIPI	Ground	MIPI ground.

Table 1. PAC7640LT Pin Description (Cont'd)

Pin No.	Symbol	Type	Description
Function	System Interface		
A5	SYS_CLK	Input	System clock input.
Function	Control Interface		
B6	I2C_SCL	Input	I^2C clock pin. Default state: input need external pull up.
C6	I2C_SDA	BiDir	I^2C data pin. Default state: input need external pull up.
Function	Data Interface		
F2	CLK_TX_P	Output	MIPI CSI-2 transmitter clock lane. MIPI D-PHY physical layer.
F3	CLK_TX_N	Output	
F4	DATA_TX_P	Output	MIPI CSI-2 transmitter data lane. MIPI D-PHY physical layer.
F5	DATA_TX_N	Output	
Function	Functional I/O		
A4	FOD_TRI	Input	Functional at FOD mode, a high pulse to trigger sending a number of frames. Default state: Hi-Z.
B3	RESETB	Input	Chip reset, active low. Default state: input with internal 100k ohm pull up.
B4	FSYNC	BiDir	Frame synchronization function. Master: output a high pulse at the end of sensor exposure. Slave: input, detect a high pulse to synchronize frame, will enter readout state immediately. Default state: Hi-Z.
D6	LED_STRB	Output	LED switch control, active high. Connect to a NMOS switch. Default state: output.
C4	TEST1	Output	For test mode Description. Default state: Hi-Z.
C5	TEST2	Output	
Function	Reserved I/O		
B5	RSV	-	Reserved. Default state: input with internal 100k ohm pull down.
C1			Reserved. Default state: Hi-Z.
D1			
D3			
D4			
D5			
E1			
E6			
F1			

Note: The default state is after applying initialization setting in PAC7640_initial.asc.

2.0 Reference Schematic

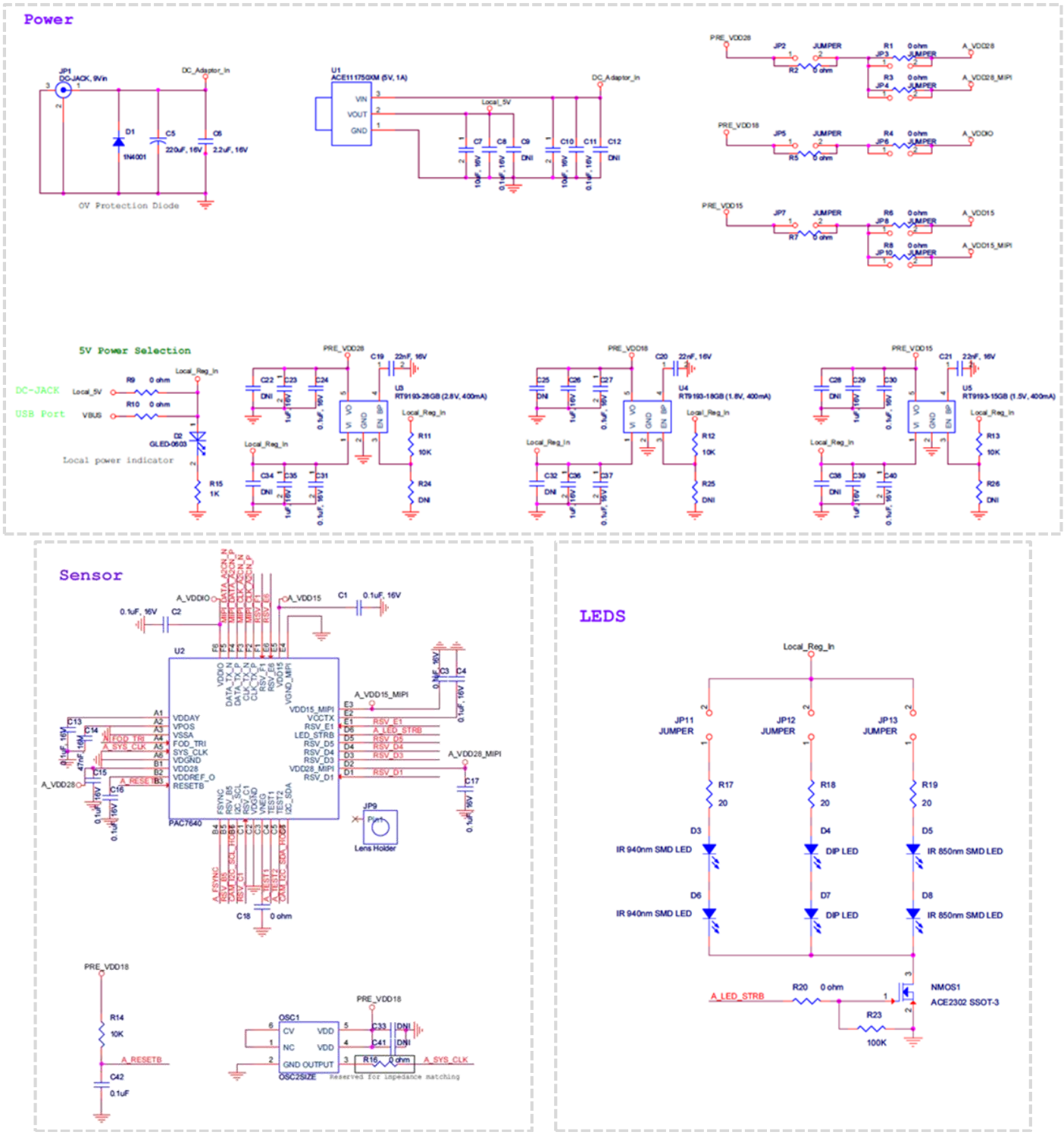

Figure 4. Reference Application Circuit

3.0 Operating Specifications

3.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Analog Voltage	V_{DD28_MAX}	-0.3	V_{DD28}+0.3	V	
Digital Core Voltage	V_{DD15_MAX}	-0.2	V_{DD15}+0.2	V	
I/O Voltage	V_{DDIO_MAX}	-0.3	V_{DDIO}+0.3	V	
I/O Pin Input High Voltage	V_{DDIO_In}	-0.3	V_{DDIO}+0.3	V	SCL, SDA
Relative Humidity	RH	0	85	%	Non-condensing, Non-biased.
ESD	ESD_{HBM}	-	2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap interval

Notes:
1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.
4. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

3.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Operating Temperature	T_A	-20	25	70	°C	
Operating Temperature at Junction	T_J	-20	-	70	°C	
Stable Image Operating Temperature at Junction	T_{SIJ}	0	-	50	°C	
Analog Supply Voltage	V_{DD28}	2.66	2.8	2.94	V	The max./min. operating voltage value is including ripples
Digital Core Voltage	V_{DD15}	1.425	1.5	1.575	V	
Digital IO Voltage	V_{DDIO}	1.71	1.8	1.89	V	
Efuse Supply Voltage	V_{DD28_efuse}	3.0	3.3	3.6	V	
Supply Noise	V_{N28}	-	-	200	mV_{p-p}	
	V_{N15}	-	-	100		
Digital IO Driving Ability	I_{DDIODR}	-	4.5	-	mA	
System clock frequency	f_{sysclk}	9.6	9.6	19.2	MHz	
System clock duty cycle	f_{sysdc}	45	-	55	%	
Frame Rate	$FR_{FullRes}$	-	-	120	fps	At Full resolution
	$FR_{HalfRes}$	-	-	240		At Half resolution

Notes: PixArt does not guarantee performance if any one temperature over the recommended operating conditions.

Table 4. Thermal Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-25	-	125	°C	
Lead-free Solder Temperature	T_P	-	-	245	°C	Refer to Error! Reference source not found.

3.3 Electrical Characteristics

Table 5. DC Electrical Specifications

Electrical Characteristics are defined under recommended operating conditions. Typical V_{DD28}=2.8V, V_{DDIO}=1.8V, V_{DD15}=1.5V, T_A = 25°C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Consumption for Single Sensor **Note:** Tested at f_{sysclk}=9.6MHz. PixArt reserves the right to update these values	P_{Rst}	-	5	-	µW	At Reset mode.
	P_{Rdy1}	-	2.7	-	mW	At Ready mode.
	P_{Slp}	-	15	158	µW	At Sleep mode.
	$P_{StmF120}$	-	65	80	mW	At Stream mode, full resolution, 120 fps, LDC Off.
	P_{StmF60}	-	33	-	mW	At Stream mode, full resolution, 60 fps, LDC Off.
	P_{StmF30}	-	17	-	mW	At Stream mode, full resolution, 30 fps, LDC Off.
	P_{StmF1}	-	1.6	-	mW	At Stream mode, full resolution, 1 fps, LDC Off.
	$P_{StmF120G}$	-	73	-	mW	At Stream mode, full resolution, 120 fps, LDC On.
	$P_{StmF60G}$	-	37	-	mW	At Stream mode, full resolution, 60 fps, LDC On.
	$P_{StmF30G}$	-	19	-	mW	At Stream mode, full resolution, 30 fps, LDC On.
	P_{StmF1G}	-	1.7	-	mW	At Stream mode, full resolution, 1 fps, LDC On.
	$P_{StmQ240}$	-	55	-	mW	At Stream mode, 1/4 resolution, 240 fps, LDC Off.
	P_{StmQ60}	-	15	-	mW	At Stream mode, 1/4 resolution, 60 fps, LDC Off.
	$P_{StmQ240G}$	-	60	-	mW	At Stream mode, 1/4 resolution, 240 fps, LDC On.
	$P_{StmQ60G}$	-	16	-	mW	At Stream mode, 1/4resolution, 60 fps, LDC On.
	P_{Fod120}		6		mW	At FOD mode, full resolution, 120 fps, LDC Off. Average power in 10 seconds.
I/O Input High Voltage	V_{IH}	0.7* V_{DDIO}	-	-	V	
I/O Input Low Voltage	V_{IL}	-	-	0.3* V_{DDIO}	V	
I/O Output High Voltage	V_{OH}	0.9* V_{DDIO}	-	-	V	@I_{OH} = 4.5mA
I/O Output Low Voltage	V_{OL}	-	-	0.1* V_{DDIO}	V	@I_{OL} = 4.5mA
Peak Analog Supply Current	I_{DDA_Peak}-	-	-	100	mA	
Peak Digital Supply Current	I_{DDD_Peak}-	-	-	100	mA	
Peak I/O Supply Current	I_{DDIO_Peak}	-	-	500	µA	

Table 6. AC Electrical Specifications

Electrical Characteristics are defined under recommended operating conditions. Typical V_{DD28}=2.8V, V_{DDIO}=1.8V, V_{DD15}=1.5V, T_A = 25°C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Power up Stream	T_{PUS}	-	-	10	ms	After all power rails reach steady level, switch to Stream mode to get first image out at 120fps.
Switch to Stream	T_{Stm}	-	-	700	µs	From Sleep/Ready mode, switch to Stream mode to get first image out.
Ready, Sleep Switch	-	-	-	700	µs	Switch between Ready, Sleep modes.
Ready, FOD Switch	-	-	-	2	clock	Switch between Ready, FOD modes.
I^2C Speed	f_{I2C}	-	100	400	kHz	
MIPI CSI-2 Data Speed	f_{MIPI}	-	249.6	-	Mbit/s	

4.0 Mechanical Specifications

4.1 Mechanical Dimension

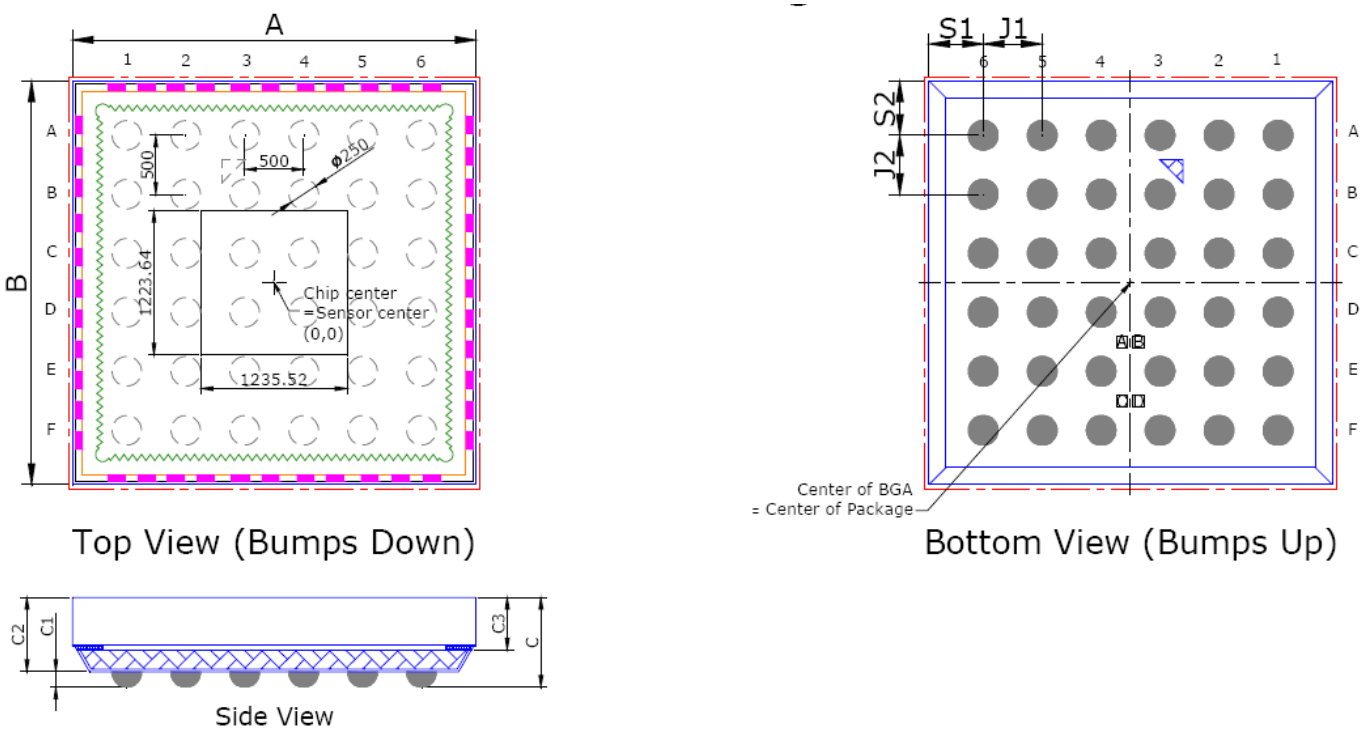

Figure 5. Package Mechanical Diagram

Table 7. Mechanical Dimension Specifications

Parameters	Symbol	Nominal	Min.	Max.	Unit
Package Body Dimension X	A	3421	3396	3446	µm
Package Body Dimension Y	B	3421	3396	3446	µm
Package Height	C	760	700	820	µm
Ball Height	C1	130	100	160	µm
Package Body Thickness	C2	630	585	675	µm
Thickness of Glass Surface to Wafer	C3	445	425	465	µm
Ball Diameter	D	250	220	280	µm
Total Pin Count	N	36	-	-	Counts
Pin Count X axis	N1	6	-	-	Counts
Pin Count Y axis	N2	6	-	-	Counts
Pin Pitch X axis	J1	500	-	-	µm
Pin Pitch Y axis	J2	500	-	-	µm
Edge to Pin Center Distance along X	S1	460.5	430.5	490.5	µm
Edge to Pin Center Distance along Y	S2	460.5	430.5	490.5	µm

4.2 Package Marking Identification

From package bottom view, the code marking printed in between ball row D to F and column 3 to 4 can be used to identify datecode of production time.

Table 8. Code Identification

Code	Description
ABCD	AB = Datecode CD = Reserved for PixArt reference

4.3 Sensor Array Overview

Table 9. Sensor Array Specification

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
X Dimension	-	-	3421	-	µm	
Y Dimension	-	-	3421		µm	
Horizontal Array Count	-	-	400	-	pixel	
Vertical Array Count	-	-	400		pixel	
Pixel Size	-	-	3	-	µm	
Package Body Thickness	-	-	-	675	µm	
CSP Ball Height	-	-	-	160	µm	
Shutter Efficiency	-	-	99.6	-	%	At 550 nm
	-	-	99.5	-	%	At 940 nm
Sensitivity	-	-	7.5	-	V/lux-sec	At 3100K (color temperature)
Quantum Efficiency	-	-	40.0	-	%	At 850 nm
	-	-	18.2	-	%	At 940 nm

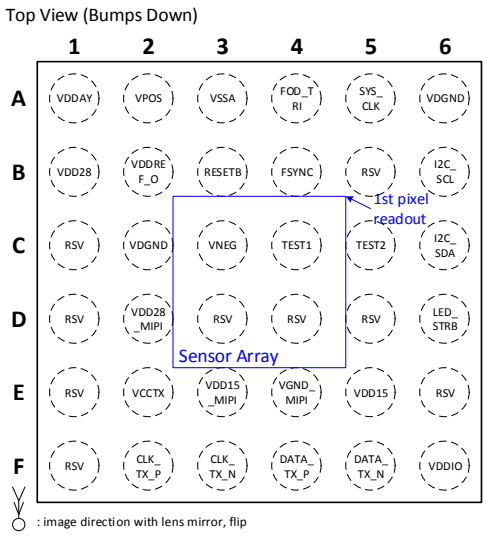

Figure 6. PAC7640LT CSP Package Overview

4.4 Packing Information

4.4.1 Chip Orientation

The chips are packed into 2-inch chip-tray with Pin 1 (A1 pin) orientation is toward the chamfer of chip tray. Refer to Figure 7. IC Orientation.

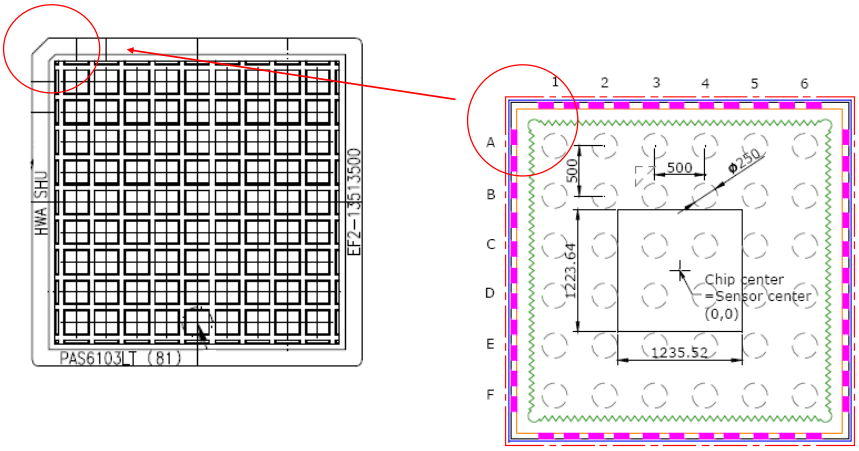

Figure 7. IC Orientation

4.4.2 Packing Capacity

Table 10. Packing Information

Parameters	Quantity	Unit	Notes
Chips per Tray	81	piece	9 x 9. Refer to Figure 7.
Trays per Stack	10	tray	Plus a top-cover on top of each stack. Refer to Figure 8
Stacks per Packing Bag	2	stacks	Packaging bag is Aluminum laminated moisture proof bag. Refer to Figure 9
Packing Bags per Packing Box	5	bag	Refer to Figure 10
Max. Chips per Packing Box	8100	piece	

Figure 8. Example of One Stack (10 Chip-Trays + 1 Cover-Tray)

Figure 9. Example of Packing Bag

Figure 10. Example of Packing Box

5.0 Power States

Table 11. Operational States

States	Functional Description
OFF	No power supply, all the voltage rails and clocks are gated.
RESET	This mode is entered when power-up sequence is executed and RESETB is held low. The sensor stays in this state as long as RESETB is held low. High on RESETB will transition the sensor to Ready mode. After power up, when the sensor is waiting for RESETB to go high, all the rails to the individual functional blocks shall be internally gated. Any time the RESETB is pulled low the sensor shall enter this mode.
READY[1]	The sensor is transitioned to this mode when RESETB is set to high. This mode can be thought of as a mode for re-initialization of the registers if they are different from the default register settings. All the rails and clocks are enabled. There is no capture or transmission of data on the MIPI lanes. All the functional blocks are enabled. Transition to Sleep can be triggered when a pre-programmed timer expires.
STREAM[1,2,3]	The sensor will enter this mode when streaming is enabled by setting R_MODE_SELECT = 1 in the ready state. The sensor will capture image and the data is transmitted on the MIPI lanes based on the settings for readout. Frame rate can be changed to any frame rate within design limitation. All the power rails and clocks are enabled as required. R_MODE_SELECT = 0 transitions the sensor back to the Ready mode. Various configurations for Stream mode like readout and synchronization settings. See more details from operation examples.
FOD[1,2,3] (Frame ON Demand)	In FOD the capture and transmission happens in response to an I/O that is controlled by the host. Transition to this state from a ready state happens when R_MODE_SELECT = 3. The FOD_TRI is configures as input before the transition. This is very similar to stream state and the only delta is in the number of frames being transmitted. In the stream state the frames are continuously transmitted based on a certain frame rate. In FOD mode even though the capture happens at the same frame rates only a few frames are captured and transmitted. The number of frames, N(up to 100), to be transmitted is programmable. While the sensor is in this mode it is waiting for a rising edge, minimum 1us hold time, on the FOD_TRI pin to begin the capture and transmission of N frames. The sensor shall transition back to ready state when R_MODE_SELECT = 0.
SLEEP[1]	This mode is entered from Ready mode either by using I^2C or autonomously. When I^2C is used the user will transition anytime by setting R_SW_PowerDown_EnH = 1. In autonomous transition happens when the timer, R_Sleep_Timer, expires. The sensor stays in this mode until the user transitions back to Ready mode by setting R_SW_PowerDown_EnH = 0. The MIPI and image capture are disabled. All the register settings initialized during the Ready mode are retained.

Notes:

1. Transition relative registers: Bank0: 0x09, 0x10, 0x14, 0x15, 0x16, 0x6D.
2. Synchronization relative registers: Bank0: 0x0B, 0x11
3. Readout relative registers: Bank1: 0x28, 0x29, 0x2A

6.0 Registers List

Table 12. Bank-0 Registers Summary

Switch to Register Bank-0 by writing 0x00 to Reg0x7F

Address	Register Function	Access	Default	Address	Register Function	Access	Default
0x00	Chip part ID	RO	0x03	0x91	LSC coefficients	R/W	0x00
0x01		RO	0x61	0x92		R/W	0x00
0x02	Chip version ID	RO	0xXX	0x93		R/W	0x08
0x03	ISP fast mapping coefficients	R/W	0x00	0x94		R/W	0x0A
0x09	Operation mode control	R/W	0x00	0x95		R/W	0x02
0x0A	Number of frames in FOD mode	R/W	0x05	0x96		R/W	0xF1
0x0B	FSYNC mode control	R/W	0x00	0x97		R/W	0xDF
0x10	Current operation mode readout	RO	0x00	0x98		R/W	0xCF
0x11	Number of frames for FSYNC skip	R/W	0x00	0x99		R/W	0xBE
0x14	Enable Sleep timer (used in READY state)	R/W	0x00	0x9A		R/W	0xBA
0x15	Sleep timer duration	R/W	0xE8	0x9B		R/W	0xBF
0x16		R/W	0x03	0x9C		R/W	0xBF
0x20	AE configuration	R/W	0x10	0x9D		R/W	0xC5
0x21	AE convergence range control	R/W	0x80	0x9E		R/W	0x42
0x22		R/W	0x08	0xA4	Bad pixel correction enable control	R/W	0x01
0x23		R/W	0x10	0xA5	BPC threshold	R/W	0x80
0x24		R/W	0x10	0xA8	Transform-domain noise reduction enable control	R/W	0x00
0x28	AE window control	R/W	0x00	0xA9	Noise reduction coefficients	R/W	0x14
0x29		R/W	0x00	0xAA		R/W	0x20
0x2A		R/W	0x64	0xAB		R/W	0x30
0x2B		R/W	0x64	0xAC		R/W	0x48
0x30	AE gain control	R/W	0x14	0xAD		R/W	0x70
0x31		R/W	0x00	0xAE		R/W	0xB0
0x32		R/W	0x00	0xAF		R/W	0xE0
0x33		R/W	0x04	0xB1		R/W	0x11
0x34	AE exposure time control	R/W	0x8C	0xB4	WOI enable control	R/W	0x00
0x35		R/W	0x00	0xB5	WOI size control	R/W	0x90
0x36		R/W	0x00	0xB6		R/W	0x01
0x37		R/W	0xEA	0xB7		R/W	0x90
0x38		R/W	0x1E	0xB8		R/W	0x01
0x39		R/W	0x07	0xB9	WOI offset control	R/W	0x00
0x3A	Max analog gain control	R/W	0x01	0xBA		R/W	0x00
0x48	Y average value in current frame	RO	-	0xBB		R/W	0x00
0x6D	Sleep mode control	R/W	0x00	0xBC		R/W	0x00
0x80	ISP enable control	R/W	0x01	0xBE	Lens distortion correction enable control	R/W	0x00
0x8A	ISP test image (test mode)	R/W	0x00				
0x90	Lens shading correction enable control	R/W	0x01				

Table 12. Bank-0 Registers Summary (Cont'd)

Address	Register Function	Access	Default	Address	Register Function	Access	Default
0xBF		R/W	0x00	0xEC	I²C Broadcast address	R/W	0x40
0xC0		R/W	0x00	0xED	I²C Slave address	R/W	0x60
0xC1		R/W	0x00	0xF0		RO	-
0xC2		R/W	0x02	0xF1		RO	-
0xC3		R/W	0x01	0xF2		RO	-
0xC4		R/W	0x03	0xF3		RO	-
0xC5		R/W	0x03	0xF4		RO	-
0xC6		R/W	0x00	0xF5		RO	-
0xC7	LDC coefficients	R/W	0xFA	0xF6		RO	-
0xC8		R/W	0xF3	0xF7	Intensity Histogram report zone0 ~ zone7	RO	-
0xC9		R/W	0xEC	0xF8		RO	-
0xCA		R/W	0xE9	0xF9		RO	-
0xCB		R/W	0xE7	0xFA		RO	-
0xCC		R/W	0xE8	0xFB		RO	-
0xCD		R/W	0xE9	0xFC		RO	-
0xCE		R/W	0x22	0xFD		RO	-
0xCF		R/W	0x10	0xFE		RO	-
				0xFF		RO	-

Table 13. Bank-1 Registers Summary

Switch to Register Bank-1 by writing 0x01 to Reg0x7F

Address	Register Function	Access	Default	Address	Register Function	Access	Default
0x00	Image horizontal size [Stream/FOD]	R/W	0x8F	0x12	ABLC upper bound	R/W	0xFF
0x01		R/W	0x01	0x13		R/W	0x03
0x02	Image vertical size [Stream/FOD]	R/W	0x8F	0x28	Readout delay configuration	R/W	0x00
0x03		R/W	0x01	0x29	Readout delay period	R/W	0xE8
0x04	Image adjustment configuration [Stream/FOD]	R/W	0x00	0x2A		R/W	0x03
0x05		R/W	0x00	0x68	Sensor black level	RO	-
0x06	Image start position [Stream/FOD]	R/W	0x04	0x69		RO	-
0x07		R/W	0x04	0x6A	Sensor power saving	R/W	0x10
0x08		R/W	0x00	0x80	Sensor setting update (_DB_ register activate)	R/W	0x00
0x09	LED strobe duration and offset control [Stream/FOD]	R/W	0x00	0x84	AE/AG manual control [Stream/FOD]	R/W	0x30
0x0A		R/W	0x00	0x85	Manual gain control [Stream/FOD]	R/W	0x00
0x0B		R/W	0x00	0x86		R/W	0x00
0x0C		R/W	0x00	0x88	Manual exposure time control [Stream/FOD]	R/W	0xDD
0x0D		R/W	0x00	0x89		R/W	0xE3
0x0E		R/W	0x00	0x8A		R/W	0x00
0x0F	LED strobe configuration [Stream/FOD]	R/W	0x10	0xBE	Frame time control [Stream/FOD]	R/W	0xEA
0x10	ABLC enable control	R/W	0xF1	0xBF		R/W	0x1E
0x11	ABLC configuration	R/W	0x00	0xC0		R/W	0x07

Table 14. Bank-2 Registers Summary

Switch to Register-Bank 2 by writing 0x02 to Reg0x7F

Address	Register Function	Access	Default
0x06	Image data output format	R/W	0x00
0x11	MIPI HS clock non-stop (test mode)	R/W	0x00
0x39	MIPI virtual channel control	R/W	0x00
0x3E	PLL setting	R/W	0x00
0x40		R/W	0x08
0x41		R/W	0x2A
0x76	Test signal output (test mode)	R/W	0x00