



# T7 DPU Products

## High Performance Programmable DPU 1/2.5/10/25/40/50/100/200/400GbE Controller

Enables several offloads, programmable compute, encryption, FPGA integration, virtualization over a single wire.

### Highlights

- Full suite of Storage features
- Full suite of Cloud features
- Full suite of data center networking features
- Full suite of data streaming features
- Full suite of encryption functions
- Embedded programmable DPU
- Embedded Arm A72 cores, accessible by user
- Adapter or micro-server functionality
- Ability to integrate with an external FPGA
- Integrated Ethernet and PCIe switch
- Software Compatible with T4, T5, and T6

### Applications

#### Datacenter Networking

- Scale out servers and NAS systems
- Consolidate LAN, SAN, and cluster networks (run InfiniBand and Fibre Channel applications on Ethernet)
- Enhanced network and server security

#### Cloud Computing

- Virtualization features to maximize cloud scaling and utilization
- Cloud-ready functional and management features
- Secure Sockets offload
- Full support for overlay products
- Seamless integration with external FPGA

#### Networked Storage

- Develop high-performance shared-storage systems providing both file and block level services
- Computational Storage
- Ethernet to the Drive
- Integrated encryption support
- NVMe Fabrics (iWARP & RoCEv2)
- NVMe/TCP (including NVMe offload)
- Very high data-integrity
- Dedupe, Compression support
- RAID, Erasure Coding support

#### High Performance Computing

- Very low latency Ethernet
- High performance RDMA support
- Increase cluster fabric bandwidth

#### Streaming Applications

- Internet attack protection
- QoS and Traffic Management
- Video streaming

#### Edge Products

- Micro Servers
- Gateways
- 5G Appliances
- Firewalls

### Overview

Chelsio's T7 is a quad port 1/2.5/10/25/50/100Gb, dual port 40/100/200Gb, or single port 400Gb Ethernet Unified Wire DPU ASIC with a PCI Express 5.0 host bus interface, optimized for storage, cloud computing, HPC, virtualization and other datacenter networking applications.

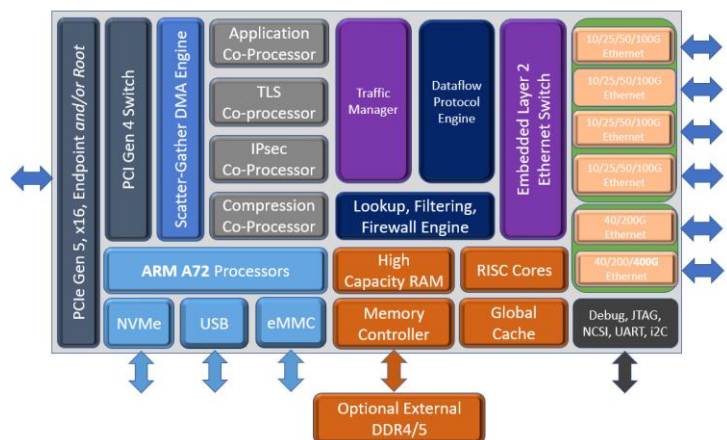
The seventh generation T7 ASIC technology from Chelsio provides the highest performance and efficiency, with dramatically lower host-system CPU communications overhead thanks to on-board hardware that offloads TCP/IP, UDP/IP, iSCSI, FCoE, Unified RDMA (RoCEv2 & iWARP), TLS/IPsec, NVMe-oF, and NVMe/TCP processing from its host system and frees up host CPU cycles for user applications. As a result, the system benefits from higher bandwidth, lower latency, and reduced power consumption.

T7 runs the predecessor T4, T5, & T6 silicon software without modification so as to enable leveraging of the user's existing software investment.

T7's architecture is Chelsio's 7<sup>th</sup> generation DPU technology road-tested across several tier-1 OEMs over the years and has evolved to support all offloads using either card memory or host memory. As a result, T7 technology can now enable a full featured DPU technology in a small memory-free package to address server and cloud applications at an aggressive price point.

### The Smart NIC Programmable DPU Solution

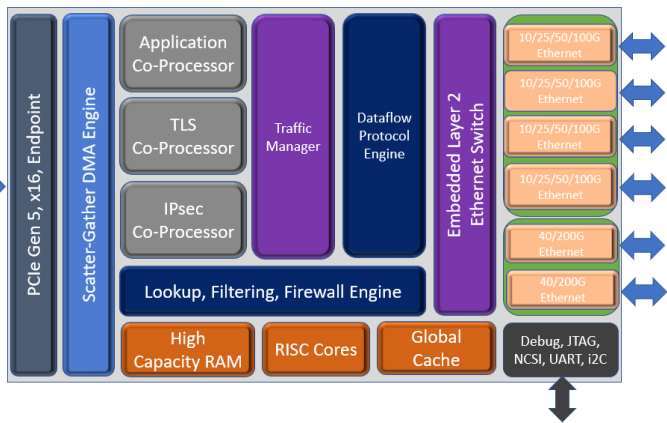
In addition to the above offloads, versions of T7 integrate 8 A72 Arm cores that are exposed to the user. These Arm cores offload the traffic to the integrated 400Gb DPU on the chip and as a result the Arm cores are available to support the user's specific application. The T7 transport engine is a programmable DPU that can offload protocol processing per connection, per-server, per-interface, while simultaneously providing complete stateless offload to traffic for non-offloaded connections (processed by operating systems stack running on host CPU). The T7 also provides a flexible direct data placement capability for regular TCP sockets, with all the benefits of zero-copy and kernel bypass without rewriting the applications. To support the Arm Cores, Chelsio provides a full development and debug software package to allow development of application specific firmware.



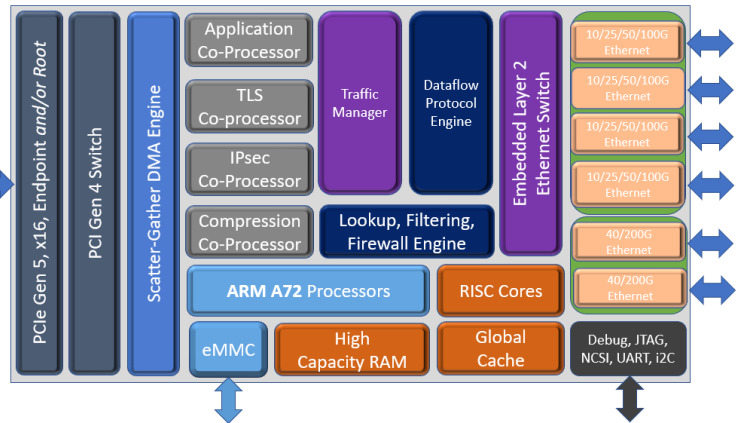
T7 Block Diagram

# Features

	T7	N7	D7	S74	S72		T7	N7	D7	S74	S72		T7	N7	D7	S74	S72
<b>Host Interface</b>						<b>Storage</b>						<b>TCP &amp; UDP Offload</b>					
PCI Express Gen5 x16	✓	✓	✓	✓	✓	iSCSI initiator and target mode stack	✓	✓	✓	✓	✓	Full TCP stack including IPv4 & IPv6	✓	✓	✓	✓	✓
Integrated PCIe switch	✓	✓	✓	✓	✓	Full FCoE offload (Initiator or Target)	✓	✓	✓	✓	✓	Extensive RFC compliance, fully featured	✓	✓	✓	✓	✓
Integrated PCIe bridge	✓	✓	✓	✓	✓	Open FCoE offload (Initiator)	✓	✓	✓	✓	✓	VLAN support up to 4096 VLAN IDs	✓	✓	✓	✓	✓
End Point or Root Complex operation	✓	✓	✓	✓	✓	T10 DIF/DIX support for iSCSI	✓	✓	✓	✓	✓	Load balancing and failover capabilities	✓	✓	✓	✓	✓
MSI-X, MSI, legacy pin interrupts	✓	✓	✓	✓	✓	NVMe-oF Offload (iWARP or RoCEv2)	✓	✓	✓	✓	✓	UDP Sockets API	✓	✓	✓	✓	✓
<b>Wire Interface</b>						<b>Security</b>						<b>High Performance RDMA</b>					
2x1/2.5/10/25/40/50/100	✓	✓	✓	✓	✓	AES 128/256 and SHA1/SHA2 offload	✓	✓	✓	✓	✓	Native RoCEv2 support	✓	✓	✓	✓	✓
4x1/2.5/10/25/50/100	✓	✓	✓	✓	✓	TLS and IPsec support	✓	✓	✓	✓	✓	Native iWARP support	✓	✓	✓	✓	✓
2x40/100/200	✓	✓	✓	✓	✓	In-line & co-processor modes	✓	✓	✓	✓	✓	All to All support	✓	✓	✓	✓	✓
1x400	✓	✓	✓	✓	✓	SM2, RSA, ECC, ECDH, ECDSA, DSA, DH	✓	✓	✓	✓	✓	<b>Data Center Features</b>					
56Gb PAM4, or 25Gb NRZ	✓	✓	✓	✓	✓	In-line IPsec & TLS for all Offload Traffic	✓	✓	✓	✓	✓	Internet Attack Protection	✓	✓	✓	✓	✓
IEEE 802.3bj (100 GbE over copper/backplane)	✓	✓	✓	✓	✓	Integrated Block or inline encryption	✓	✓	✓	✓	✓	PFC, DCB, CEE	✓	✓	✓	✓	✓
IEEE 802.3cd (50/100/200 GbE)	✓	✓	✓	✓	✓	True Random Number Generator	✓	✓	✓	✓	✓	Time stamping support	✓	✓	✓	✓	✓
IEEE 802.3ba (40/100 GbE)	✓	✓	✓	✓	✓	Secure firmware update	✓	✓	✓	✓	✓	<b>Embedded Processors</b>					
IEEE 802.3ae (10 GbE)	✓	✓	✓	✓	✓	Hardware Root of Trust support	✓	✓	✓	✓	✓	ARM A72 Cores, 2MB L2 Cache	8	4			
IEEE 802.3az Energy Efficient Ethernet	✓	✓	✓	✓	✓	<b>Cloud &amp; Virtualization</b>						RISC Cores	8	8	4	4	1
IEEE 802.3z (1GbE)	✓	✓	✓	✓	✓	NVMe Virtualization/Emulation	✓	✓				400Gb DPU Core	1	1	1	1	1
IEEE 802.1p Priority	✓	✓	✓	✓	✓	Virt-IO	✓	✓				<b>Management and Other Interfaces</b>					
IEEE 802.1Q VLAN Tagging	✓	✓	✓	✓	✓	OVS Offload	✓	✓	✓	✓	✓	USB 2.0 Host Mode	✓				
IEEE 802.1Qbg EVB/VEPA	✓	✓	✓	✓	✓	Seamless integration with external FPGA	✓	✓	✓	✓	✓	UART	✓	✓	✓	✓	✓
IEEE 802.1BR Bridge Port Extension	✓	✓	✓	✓	✓	Inband Telemetry	✓	✓	✓	✓	✓	eMMC 4.51	✓	✓			
IEEE 802.1Qau Congestion Notification	✓	✓	✓	✓	✓	NVGRE, VXLAN and GENEVE support	✓	✓	✓	✓	✓	NVMe Gen 4, x2	✓				
IEEE 802.3x Flow Control	✓	✓	✓	✓	✓	PCI-SIG SR-IOV, 256 VF, 8 PF	✓	✓	✓	✓	✓	NC-SI	✓	✓	✓	✓	✓
IEEE 802.3ad Load-balancing and Failover	✓	✓	✓	✓	✓	264 port virtual switch	✓	✓	✓	✓	✓	SPI Flash	✓	✓	✓	✓	✓
Ethernet II and 802.3 encapsulated frames	✓	✓	✓	✓	✓	EVB, VEPA, Flex10, VNTag	✓	✓	✓	✓	✓	I2C, MDIO, GPIO, JTAG	✓	✓	✓	✓	✓
Multiple MAC addresses per interface	✓	✓	✓	✓	✓	512 MAC addresses	✓	✓	✓	✓	✓	PLDM, MCTP (SMBus or PCIe), RBT	✓	✓	✓	✓	✓
Jumbo Frames up to 9.6 Kbytes	✓	✓	✓	✓	✓	NAT Offload	✓	✓	✓	✓	✓	<b>Boot Facilities</b>					
ITU-T G.8262, Sync-E	✓	✓	✓	✓	✓	<b>Streaming</b>						iSCSI, FCoE, PXE, UEFI	✓	✓	✓	✓	✓
<b>Stateless Offloads</b>												Secure Boot	✓	✓	✓	✓	✓
TCP/UDP checksum offload for IPv4 & IPv6	✓	✓	✓	✓	✓							<b>Host Interface</b>					
TSO, LSO, and GSO for IPv4 & IPv6	✓	✓	✓	✓	✓							PCI Express Gen5 x16	✓	✓	✓	✓	✓
VLAN filtering, insertion & extraction	✓	✓	✓	✓	✓							Integrated PCIe switch	✓	✓	✓	✓	✓
Packet filtering and attack protection	✓	✓	✓	✓	✓							Integrated PCIe bridge	✓	✓	✓	✓	✓
Nanosecond granularity 64b timestamping	✓	✓	✓	✓	✓							End Point or Root Complex operation	✓	✓	✓	✓	✓
Ethernet Routing (packet header rewrite)	✓	✓	✓	✓	✓							MSI-X, MSI, legacy pin interrupts	✓	✓	✓	✓	✓
Packet Tracing and Packet Sniffing	✓	✓	✓	✓	✓							<b>Wire Interface</b>					
<b>Management and Other Interfaces</b>												2x1/2.5/10/25/40/50/100	✓	✓	✓	✓	✓
USB 2.0 Host Mode	✓											4x1/2.5/10/25/50/100	✓	✓	✓	✓	
UART	✓	✓	✓	✓	✓							2x40/100/200	✓	✓	✓	✓	
eMMC 4.51	✓	✓										1x400	✓	✓	✓	✓	
NVMe Gen 4, x2	✓											56Gb PAM4, or 25Gb NRZ	✓	✓	✓	✓	
NC-SI	✓	✓	✓	✓	✓							IEEE 802.3bj (100 GbE over copper/backplane)	✓	✓	✓	✓	
SPI Flash	✓	✓	✓	✓	✓							IEEE 802.3cd (50/100/200 GbE)	✓	✓	✓	✓	
I2C, MDIO, GPIO, JTAG	✓	✓	✓	✓	✓							IEEE 802.3ba (40/100 GbE)	✓	✓	✓	✓	
PLDM, MCTP (SMBus or PCIe), RBT	✓	✓	✓	✓	✓							IEEE 802.3ae (10 GbE)	✓	✓	✓	✓	
<b>Boot Facilities</b>												IEEE 802.3az Energy Efficient Ethernet	✓	✓	✓	✓	
iSCSI, FCoE, PXE, UEFI	✓	✓	✓	✓	✓							IEEE 802.3z (1GbE)	✓	✓	✓	✓	
Secure Boot	✓	✓	✓	✓	✓							IEEE 802.1p Priority	✓	✓	✓	✓	



S7 Block Diagram



D7 Block Diagram

## Ordering Information

	T7ASIC	N7ASIC	D7ASIC	S74ASIC	S72ASIC
Card Memory	Optional	Optional	-	-	-
Typical Power	17-22W	17W	10-14W	12W	8W
Package Size (0.8mm pitch)	31mm	31mm	21mm	21mm	21mm

## Physical & Environmental

- Fully RoHS Compliant
- Operating Temp: 0° to 55° C or 32° to 131° F
- Operating Humidity: 5 to 95%
- Airflow: 200 LFM

# Applications

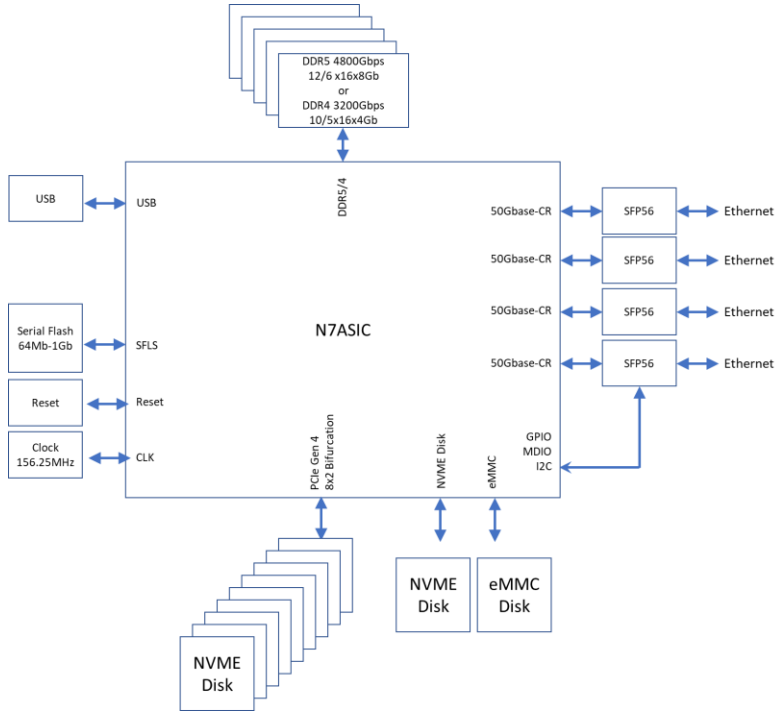


Figure 2 – Single Chip Server Application

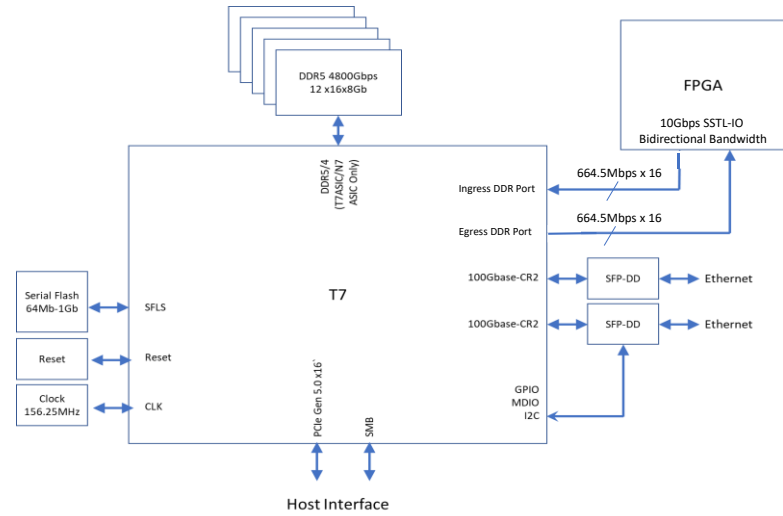


Figure 1 – iNIC Application

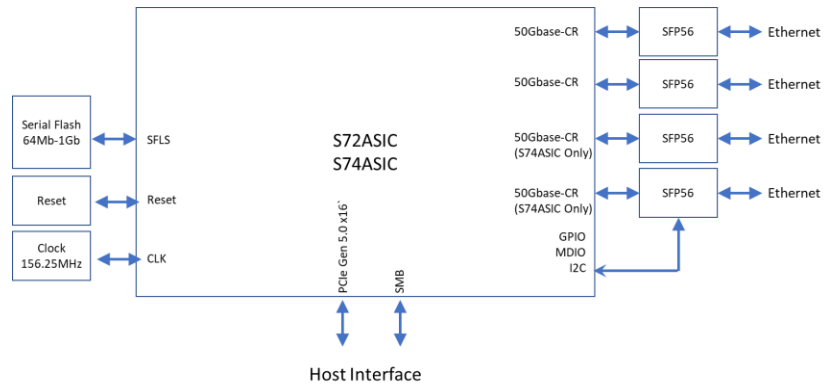


Figure 3 – Standard NIC Application

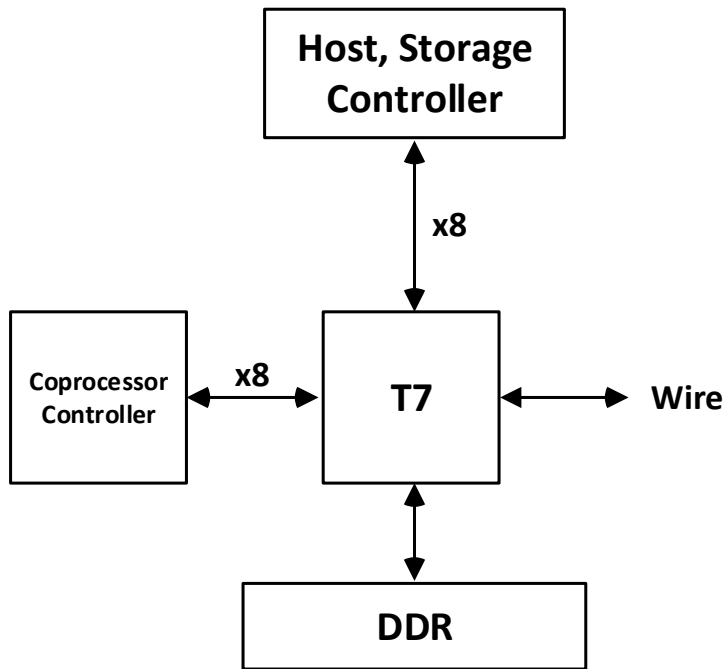


Figure 4 – Generalized Bridge

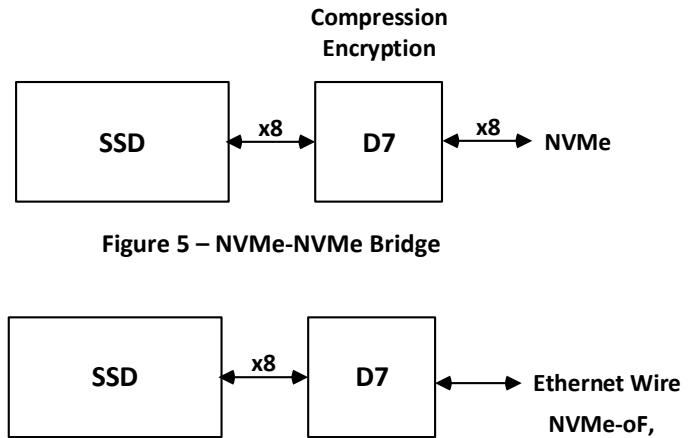


Figure 5 – NVMe-NVMe Bridge

Figure 6 – NVMe-Ethernet Bridge

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH CHELSIO PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN CHELSIO'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, CHELSIO ASSUMES NO LIABILITY WHATSOEVER, AND CHELSIO DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND OR USE OF CHELSIO PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. CHELSIO PRODUCTS ARE NOT INTENDED FOR USE IN MEDICAL, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS. CHELSIO MAY MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE.

Copyright © 2022 - Chelsio Communications - All rights reserved.